

VOLTAGE SAG AND SWELL MITIGATION USING HYSTERESIS BAND CONTROLLED THREE-PHASE TWELVE SWITCH CONVERTER BASED DVR

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Abstract- This paper proposes hysteresis band controller based three-phase voltage source converter with twelve switches. The proposed common mode dc voltage source, three-levels converter is applied in DVR systems for voltage sag and swell mitigation and harmonic reduction. Hysteresis band controlled converters have the following merits; simple to control, robust control and rapid dynamic response for distorted voltage, voltage dip and swell conditions. To minimize zero sequence components, three single-phase transformers are employed in place of single three-phase transformer. System reliability and flexibility are maximized when single-phase transformers are utilized. At the point of common coupling (PCC), the transformers are connected directly (devoid of delta or star connections) to the grid so as to improve voltage compensations and harmonic reduction. Power circuit of the proposed converter and its control circuit are modelled in MATLAB Simulink, produced simulation results validates the performance of the proposed converter.

Keywords: Dynamic Voltage Restorer, Hysteresis Band Controller, Twelve Switch Converter, Voltage Sag, SOGI.

1. INTRODUCTION

Power quality issues caused by frequency and voltage are increased when irregular renewable energy sources are harnessed for electric power production via distributed generations (DGs). As a result, distribution systems may face fluctuations and voltage distortions. Network impedances may cause currents of non-linear loads to generate non sinusoidal voltage drops. Furthermore, short-circuit faults may introduce voltage sag and swell drawbacks.

By definition, voltage sag is an abrupt reduction in rms voltage while voltage swell is an abrupt rise in the rms voltage, the fall and rise duration of nominal voltage for voltage sag and swell conditions are between 10%-90% and 110%-180% respectively according to IEEE standards [1-4]. DVR (dynamic voltage restorer), a voltage compensating device, which is widely accepted in industry, is the solution for mitigating these power quality

issues [5-6]. Stepped output voltage feature of DVR enables reduction or elimination of harmonic content [7].

The control mechanism of the dynamic voltage restorer drives a converter as an auxiliary regulatory voltage source operating in conjunction with the supply lines. The DVR exhibits high resistance to the load harmonics or source and zero impedance at fundamental frequency depending on the control capabilities of the control mechanism.

An integral component of the DVR is the converter. By employing appropriate control technique, converter operation directly relates to dynamic operation, steady state and cost of device. Some example of commonly used control techniques is carrier based PWM, open loop controlled based SPWM (sine pulse width modulation) [8]. Sub-oscillation carrier based PWM and SVPWM (space vector PWM) have the error drawback of steady state tracking which is caused by PI controller and open loop behaviors' respectively [9-10]. Additionally, closed loop techniques such as dead-beat, state feedback and combined feedforward and feedback require intensive computational methodologies [11-13]. With regard to control characteristics, robustness is archived with Stationary-frame control [14]. The response time of these control techniques is relatively slow, furthermore, complex computation and detailed system data are required.

The above mentioned drawbacks are resolved by employing a closed loop control technique which is simple to implement, has fast response time and control robustness, this methodology is referred to as Hysteresis band control. Current and voltage controllers are two types of Hysteresis band control. Hysteresis current control has been proven to provide fast response but it's not suitable for DVR applications [15]. Hysteresis voltage control is suitable for DVR applications because voltage injection is directly required.

This paper proposes hysteresis band controller based three-phase voltage source converter with twelve switches. The proposed common mode dc voltage source, three levels converter is utilized in DVR systems for voltage mitigations. New voltage sag and swell detection technique is also presented. To minimize zero sequence

components, 3 single-phase transformers are employed rather than one three-phase transformer. Also, system reliability and flexibility are maximized when single-phase transformers are utilized.

The proposed twelve switch hysteresis band-controlled converter has the following advantages:

- Simple to control
- Control robustness
- Acceptable harmonic content.
- Fast dynamic response for distorted voltage, voltage dip and swell conditions.

2. GENERALIZED SINGLE-PHASE DVR MODELLING

Figure 1 shows a single-phase dynamic voltage restorer fed by a four switch H-bridge inverter. The inverter is connected in series to the grid by a transformer at the point of common coupling. The transformers functions as the injecting device and also provide galvanic isolation. As shown in Figure 1, there are four voltages i.e., v_D , v_G , v_L and v_{IN} which corresponds to DVR voltage or injected voltage, grid voltage, load voltage and converter or inverter output voltage accordingly. Because of symmetric features of three-phase DVR topologies, analysis of one phase is valid for all other phases. Hence generalized analysis of the DVR of Figure 1 is valid for the proposed three-phase DVR. Analyzing Figure 1 by KVL produces equation (1) expression below:

$$v_D = v_L - v_G \tag{1}$$

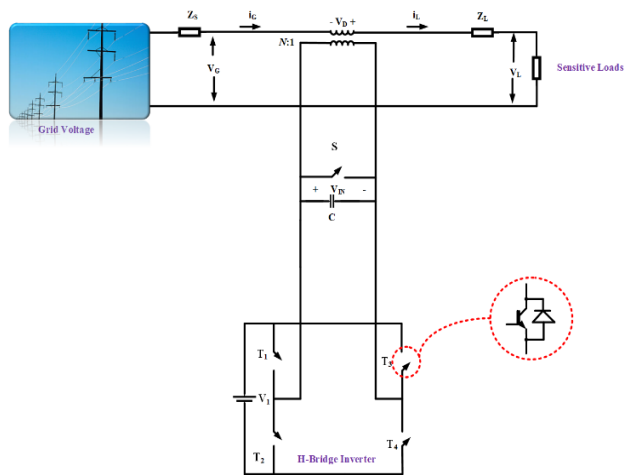


Figure 1. Hysteresis voltage controlled DVR

The instantaneous relationship between the three voltages (v_G , v_{IN} and v_D) are expressed by equations (2) and (3):

$$v_G = \frac{v_{IN}}{t_r} \tag{2}$$

$$v_{IN} = \frac{v_D}{a} \tag{3}$$

where,

t_r is the transfer ratio of the inverter,

a is the transformers secondary turns ratio.

Based on equations (2) and (3), the grid voltage and DVR voltage relates by equation (4):

$$v_D = a \times t_r \times v_G \tag{4}$$

The single-phase sinusoidal voltages for the DVR system is expressed below by equations (5)-(7):

$$V_{IN,max} = t_r V_{G,max} \tag{5}$$

$$V_{D,max} = a V_{IN,max} \tag{6}$$

$$V_{D,max} = a t_r V_{G,max} \tag{7}$$

During voltage sag or swell disturbance, the inverter output voltage for compensation is expressed by:

$$v_{IN} = V_{IN,max} \sin(\omega t + \varphi) \tag{8}$$

where, $V_{IN,max}$ is the maximum voltage of the fundamental component and φ is the phase angle of the DVR voltage and defined for sag and swell disturbance as:

$$\begin{cases} \varphi = 0, & \text{During sag disturbance} \\ \varphi = 180, & \text{During swell disturbance} \end{cases} \tag{9}$$

Considering the above equations, the compensating voltage percentage (V_p) during voltage sag and voltage swell disturbances are expressed equations (10)-(11) [16]:

$$V_{P,SAG} = \frac{V_{L,max} - V_{G,max}}{V_{L,max}} \tag{10}$$

$$V_{P,SWELL} = \frac{V_{G,max} - V_{L,max}}{V_{L,max}} \tag{11}$$

3. TWELVE SWITCH VSI CONVERTER

Figure 2 illustrates the power circuit of twelve-switch voltage source converter. As depicted by the Figure 1, only one dc voltage source is required by the converter. Twelve unidirectional semiconductor power switches from voltage point of view are required. One IGBT and antiparallel connected diode constitute each power switch of the converter. The presented topology is a 3-level converter, i.e., the maximum level of output voltage that can be generated is 3 which is expressed by equation (1).

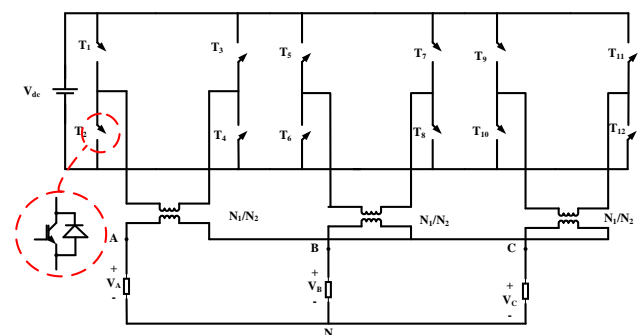


Figure 2. Hysteresis voltage controlled DVR

The switching scheme of the presented topology is illustrated by Table 1. as shown by Table 1, each phase is controlled independently to generated the required magnitude of output voltage. Positive output voltages are generated by left to right diagonal gating of power switches i.e., T_1 and T_4 are gated on to generate positive V_{dc} while right to left diagonal gating of power switches generates negative output voltage i.e., T_2 and T_3 are gated

on to generate negative V_{dc} . Equations (12) to (15) represents the power circuit details and equations of the twelve-switch converter of Figure 2.

$$N_{DC} = 1 \tag{12}$$

$$N_{1\phi, Level} = 3 \tag{13}$$

$$V_{O,Max} = V_{DC} \tag{14}$$

$$N_{Switches} = 12 \tag{15}$$

$$N_{Driver} = 12 \tag{16}$$

The three-phase voltage of Figure 2 are expressed by

$$\begin{cases} V_{AB} = V_{AN} - V_{BN} \\ V_{BC} = V_{BN} - V_{CN} \\ V_{CA} = V_{CN} - V_{AN} \end{cases} \tag{17}$$

Table 1. Switching pattern

| State | Switches | V_A | Switches | V_B | Switches | V_C |
|-------|--|-----------|--|-----------|---|-----------|
| I | T ₁ , T ₄ | V_{dc} | T ₅ , T ₈ | V_{dc} | T ₉ , T ₁₂ | V_{dc} |
| II | T ₁ , T ₃ T ₂ , T ₄ | 0 | T ₅ , T ₇ T ₆ , T ₈ | 0 | T ₉ , T ₁₁ T ₁₀ , T ₁₂ | 0 |
| III | T ₂ , T ₃ | $-V_{dc}$ | T ₆ , T ₇ | $-V_{dc}$ | T ₁₀ , T ₁₁ | $-V_{dc}$ |

4. PROPOSED TWELVE SWITCH CONVERTER BASED DVR

Figure 1 depicts system architecture of the proposed DVR based hysteresis band controller based three-phase voltage source converter with twelve switches. By utilizing only one dc source for the proposed topology, voltage control for multiple dc sources which requires extra control technique is eliminated. The ac output section of each phase of the proposed topology is connected to the supply lines at PCC via a single-phase transformer, an LC filter is placed between the inverter output and PCC.

These transformers are commonly referred to as injection transformers and are connected in series to the supply or utility. In connecting the secondary section of the transformer to the converter output, delta or star connections are utilized. However, this is not applicable because of the converter type; twelve switches. Hence direct connection of the transformer and converter is done as shown in Figure 1. These types of converters are widely used because they provide effective regulation on zero sequence components which caters for voltage sag in single-phase and unbalanced voltage. Consequently, direct converter-transformer connection of the proposed DVR topology is essential in unbalanced utility voltage compensations.

4.1. Hysteresis Voltage Band Control

Analysis of hysteresis voltage band controlled DVR is provided in this section. Selecting appropriate reference computation technique determines the DVRs reference voltage V_{ref} . The synthesized reference voltage by the converter is injected in series to the grid as case of all DVRs. Hysteresis voltage control enables the application of suitable switching patterns for the converter. Let X represent the hysteresis band, therefore upper and lower boundaries are given by Equations (18) and (19) respectively.

$$V_{ref} + X \tag{18}$$

$$V_{ref} - X \tag{19}$$

The converters output voltage is made to tracks the reference voltage within the upper and lower boundaries of the band. If V_{DVR} fall below the lower boundary, positive ac voltage is generated by gating switches T₁ and T₄, T₅ and T₈, T₉ and T₁₂ for phases A, B and C respectively. If V_{DVR} rises above the upper boundary, negative ac voltage is generated by gating switches T₂ and T₃, T₆ and T₇, T₁₀ and T₁₁ for phases A, B and C respectively. Using phase A for explanation purposes, the control sequence of the converter is given by:

$$\text{when } V_{DVR} > V_{ref} + X : \tag{20}$$

Switches T₁ and T₄ are OFF and T₂ and T₃ are ON

$$\text{when } V_{DVR} < V_{ref} - X : \tag{21}$$

Switches T₁ and T₄ are ON and T₂ and T₃ are OFF

Figure 3 shows the band controller with the upper and lower boundaries, the reference voltage and DVR voltage. The discretional DVR reference voltage is between the upper and lower boundary and depicted by dashed lines. Three references voltages V_{ref1} , V_{ref2} and V_{ref3} occur at time intervals t_1 , t_2 and t_3 , accordingly. By subtracting and adding hysteresis band from/to reference voltages, the lower and upper boundaries are created. Positive reference voltage is tracked when switches T₁ and T₄ are gated ON while switches T₂ and T₃ remains OFF, this occurs during time interval t_1-t_2 . This puts V_{dc} to the converter output hence DVR actual voltage rises from $V_{ref}-X$ to $V_{ref2}+X$ through V_{ref} .

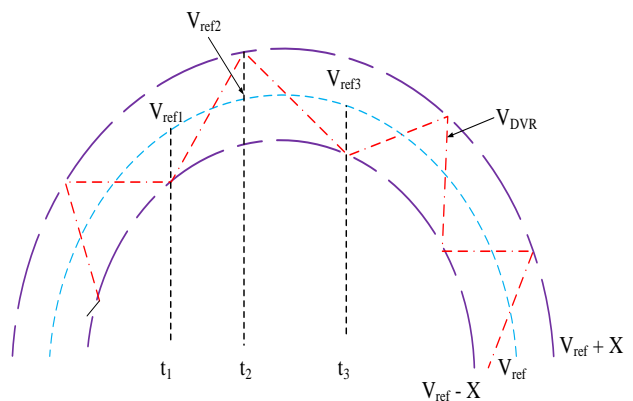


Figure 3. Hysteresis voltage controlled DVR

If the DVR voltage crosses the upper boundary $V_{ref2}+X$, it has to brought down to the lower boundary, this occurs during the time intervals t_2 to t_3 . Negative voltage is generated during this time by gating switches T₂ and T₃ while switches T₁ and T₄ remains in the OFF state. Voltage tracking determines the ON or OFF states of the switches (IGBTs). However, the direction of converter current determines the switching states of the switches (diodes and IGBTs). Table 2 shows detailed switching states of all devices during for positive and negative voltage tracking and converter current states.

Table 2. Hysteresis voltage controlled switching operation

| POSITIVE REFERENCE VOLTAGE | | | | NEGATIVE REFERENCE VOLTAGE | | | |
|--------------------------------|--|--------------------------------|--|--------------------------------|--|--------------------------------|--|
| Positive converter current | | Negative converter current | | Positive converter current | | Negative converter current | |
| ON Devices | OFF Devices | ON Devices | OFF Devices | ON Devices | OFF Devices | ON Devices | OFF Devices |
| T ₁ -T ₄ | T ₂ -T ₃ D ₁ -D ₄ D ₂ -D ₃ | D ₂ -D ₃ | D ₂ -D ₃ T ₁ -T ₄ T ₂ -T ₃ | D ₁ -D ₄ | D ₂ -D ₃ T ₁ -T ₄ T ₂ -T ₃ | T ₂ -T ₃ | T ₁ -T ₄ D ₁ -D ₄ D ₂ -D ₃ |

4.2. Detection of Voltage Sag/Swell and Harmonic

Second-order generalized integrator (SOGI) is utilized in deriving fundamental harmonics of the individual sources at a frequency of 50Hz. SOGI block for phase A of the proposed topology is illustrated by Figure 4. Voltage sensor initially detects individual source voltages vs(t) which is then processed by SOGI. Equations (22)-(23) show SOGI characteristic transfer function [14].

$$F_1(s) = \frac{\bar{v}_{s\alpha}(s)}{v_s(s)} = \frac{K\omega s}{s^2 + K\omega s + \omega^2} \tag{22}$$

$$F_2(s) = \frac{\bar{v}_{s\beta}(s)}{v_s(s)} = \frac{K\omega s}{s^2 + K\omega s + \omega^2} \tag{23}$$

where,

- K is algorithm damping factor
- V_s is source voltage
- ω is angular frequency

Application of SOGI algorithm together with frequency locked loop (FLL) or phase locked loop (PLL) enables the determination of the input waveforms frequency [17-19]. As shown in Table 2, the angular frequency for this work is tuned to 314 rad/s. using angular frequency of 2π×50 rad/s and damping factor of 1, analysis of Bode diagrams were investigated for system (1) and (2) in [14].

In this work, the same parameters are utilized. As indicated by the diagrams in [14], the first system F₁(s) is

a band-pass filter while the second system F₂(s) is a low-pass filter. This is due to that fact that; frequency of the source waveform is equivalent to the angular (tuned) frequency. The waveform of the source voltage and SOGI output waveform are equal in amplitude and phase. Harmonic components of the input voltage are determined by subtracting source voltage from voltage generated by SOGI as shown by:

$$v_s(t) = \bar{v}_s(t) - v_s(t) \tag{24}$$

Moreover, fluctuating voltage amplitudes for voltage sg and swell for each phase voltages V_{sa}, V_{sb}, V_{sc} are determined by amplitude detector then dividing amplitude of the source voltage as shown by:

$$\sin(\omega t + \varphi) = \frac{v_s(t)}{V_s} \tag{25}$$

Unity sine functions are derived for each phase at this stage which alternates between +V and -V. Lastly, reference load voltages are computed by multiplication with 230√2 as shown by:

$$v_L^*(t) = 230\sqrt{2} \sin(\omega t + \varphi) \tag{26}$$

It is evident at 230√2 level, the reference load voltages are stabilized. The load voltage variations or difference (Δv_L) in individual phase is determined by subtracting reference voltage in Equation (26) from measured input voltage as shown by:

$$\Delta v_L(t) = v_s(t) - v_L^*(t) \tag{27}$$

Total reference compensating voltage for individual phases is derived by addition of harmonic component voltages derived in Equation (24) to the voltage difference derived in Equation (27) yields the equation below:

$$v_c^*(t) = v_s(t) + \Delta v_L(t) \tag{28}$$

Lastly, the total reference injecting (compensation) voltage for individual phases is used as the reference voltage for the hysteresis voltage controller (v_{ref}) as indicated above.

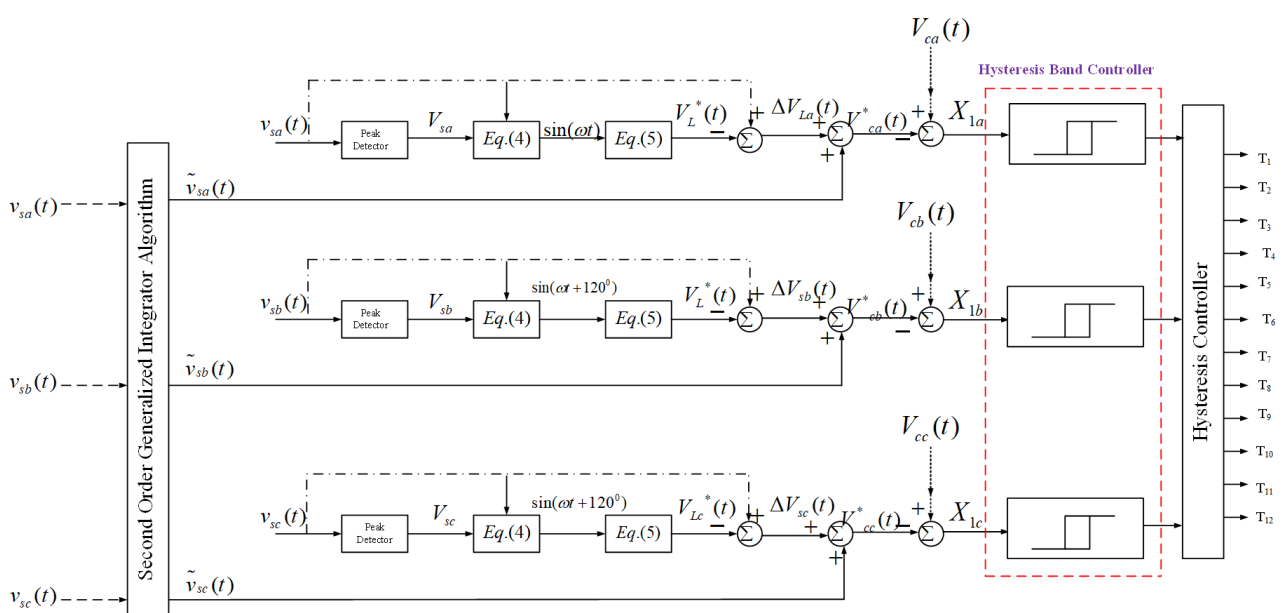


Figure 4. Block diagram of hysteresis band control unit

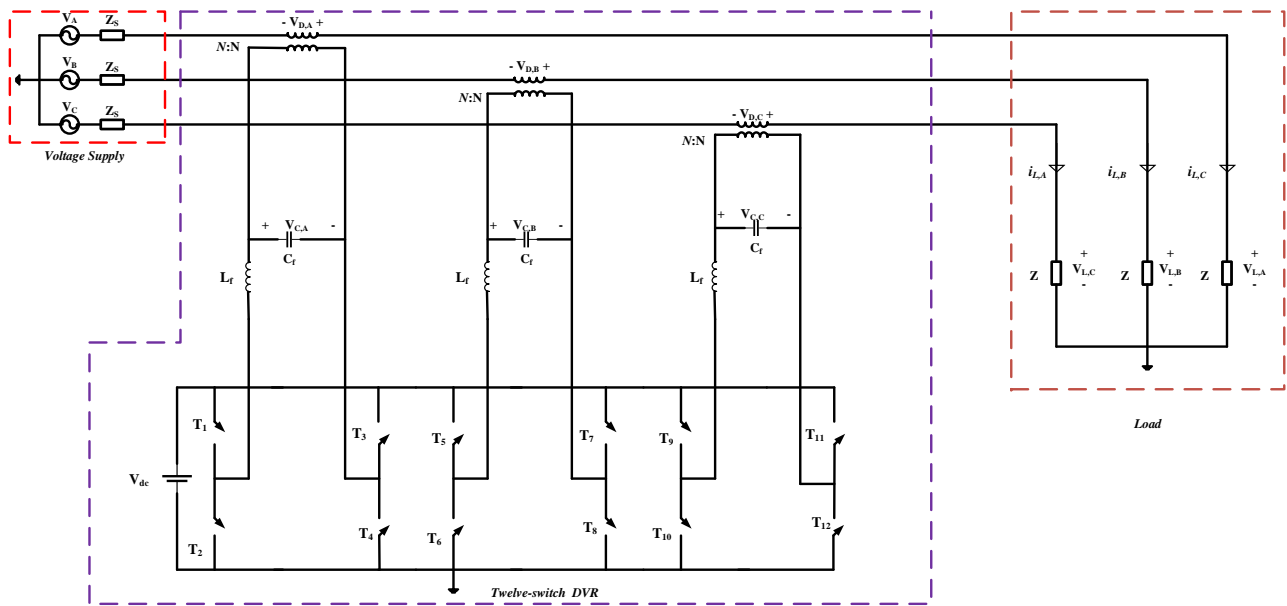


Figure 5. Hysteresis voltage controlled DVR

3. SIMULATION RESULTS

In this section, simulation results of the proposed hysteresis band controller based DVR with twelve-switch three-phase voltage source converter is presented. The power circuit of the proposed converter of Figure 5 and its control architecture of Figure 4 are designed in MATLAB Simulink to investigate its performance under voltage sag, voltage swell and harmonic conditions. Table 3 shows the system parameters utilized in simulation.

Table 3. Simulation Parameters

| Parameter | Symbol | Magnitude |
|-------------------------|----------|--------------------|
| Grid voltage | V_s | 230 V, 50 Hz |
| Switching frequency | f_s | 10 kHz |
| Inductance | L | 0.3 mH |
| Sampling time | T_s | 35 μ s |
| Transformer turns ratio | n | 1:1 |
| Capacitance | C | 150 μ F |
| SOGI gain | K | 1 |
| DC-link voltage source | V_{dc} | 600 V |
| Load | RL | 4 Ω , 10 mH |

Simulation results of the proposed hysteresis band controller based three-phase voltage source converter with

twelve switches are illustrated by Figure 6 to Figure 9. Figure 6 shows three-phase grid waveforms, between the time intervals of $0 \leq t \leq 0.05$ sec, the three-phase waveforms are equivalent to the rated grid voltage waveforms, with respect to the magnitude and phase.

However, voltage sag occurs in the time intervals of $0.05 \leq t \leq 0.1$ sec for phases A and B as indicated by the waveform of Figure 6. The peak voltage for each phase is at rated value of 325V, due to voltage sag conditions, the peak voltage of phases A and B are reduced to approximately 230V and 180V accordingly. Therefore, positive 95V and 140V are injected by the DVR to compensate voltage sag conditions in phases A and B respectively. To compensate voltage swell conditions, negative voltage of required magnitude and phase is injected for compensations. Figure 7 illustrates the three-phase load voltage waveform after injecting required voltages to mitigate voltage sag conditions of phases A and B, as can be seen, all three waveforms have the appropriate rated voltage waveforms with respect to magnitude and phase. Figure 10 shows the FFT of proposed topology with THD of 3.11%.

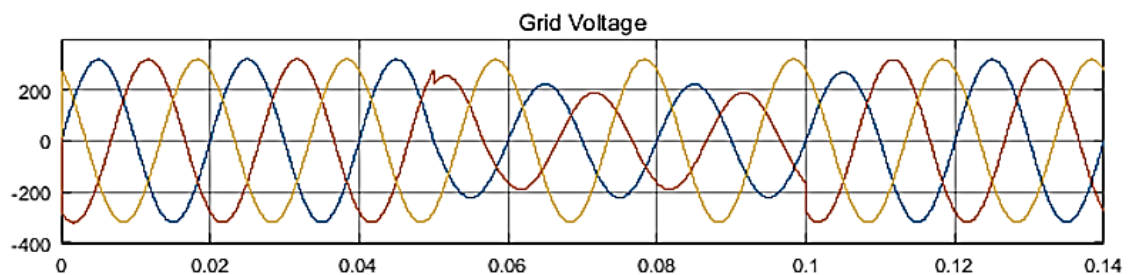


Figure 6. Three-phase grid voltage waveform

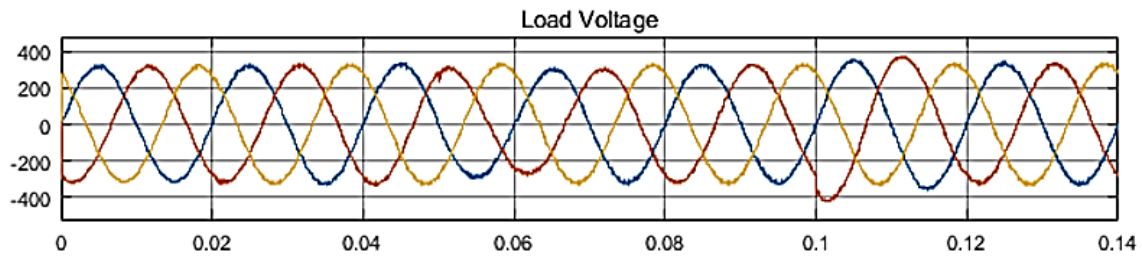


Figure 7. Three-phase load voltage waveform

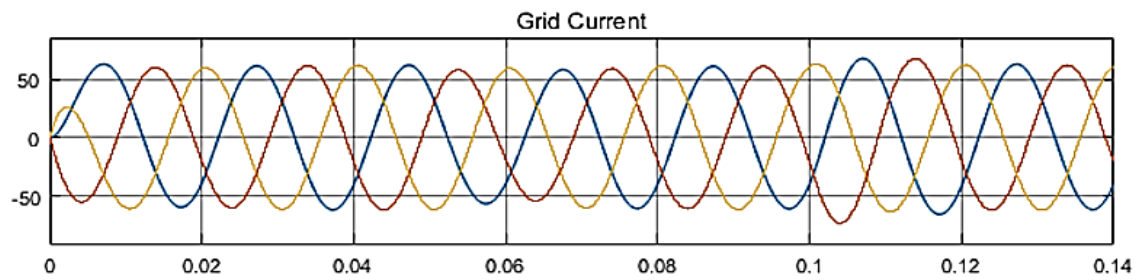


Figure 8. Three-phase waveform of grid current

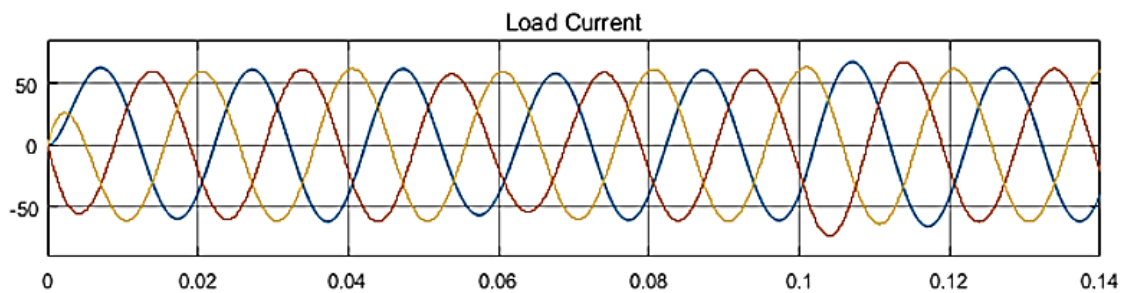


Figure 9. Three-phase load current waveform

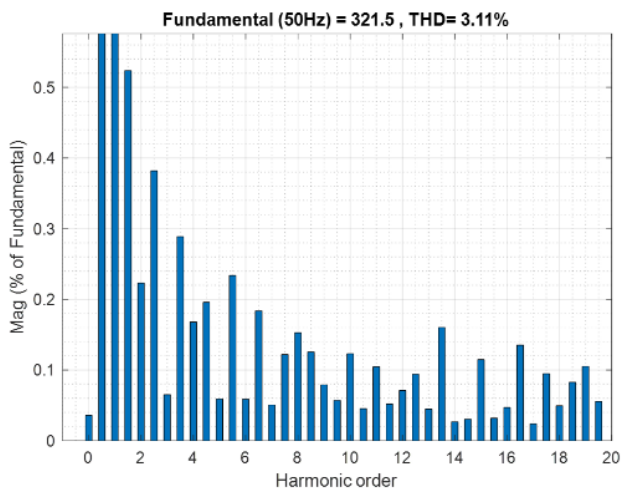


Figure 10. FFT of proposed topology

6. CONCLUSIONS

In this work, hysteresis band controller based three-phase voltage source converter with twelve switches was introduced for application in DVR systems to mitigate voltage sag and swell disturbances. The proposed topology was verified under voltage sag and swell conditions by implementing a modelled architecture in Matlab Simulink. Simulation results of sag conditions shows the proposed topology can mitigate voltage disturbances such as voltage

sag and swell. Also, harmonic content of the proposed topology is significantly minimized because of the use of the twelve-switch multilevel inverter and LC filter. The proposed hysteresis band controlled twelve switch converter is ideally suitable for DVR applications because of control simplicity and robustness in control and minimum THD content of less than 5%.

REFERENCES

- [1] M. Ramasamy, S. Thangavel, "Experimental Verification of PV Based Dynamic Voltage Restorer with Significant Energy Conservation", *Electrical Power and Energy Systems*, vol. 49, pp. 296-307, 2013.
- [2] S. Biricik, H. Komurcugil, M. Basu, "Sliding mode control strategy for three-phase DVR employing twelve-switch voltage source converter", *The 41st Annual Conference of the IEEE Industrial Electronics Society (IECON 2015)*, pp. 000921-000926, 2015.
- [3] L. Diaz, L. Ramirez, J. Fabregas, "Green Logistics in Off-Grid Renewable Energy Projects for the Rural Localities", *International Journal on Technical and Physical Problems of Engineering (IJTPE)*, Iss. 48, Vol. 13, No. 3, pp. 119-124, September 2021.
- [4] A. Gill, A. Choudhary, H. Bali, A. Kalwar, "Impact of DGS Power Factor on Voltage Profile and Power Losses of Distribution Network", *International Journal on Technical and Physical Problems of Engineering (IJTPE)*, Iss. 47, Vol. 13, No. 2, pp. 1-6, June 2021.

[5] N.G. Jayanti, M. Basu, I. Axente, K. Gaughan, M.F. Conlon, "Sequence analysis based DSP controller for Dynamic Voltage Restorer (DVR)", IEEE Power Electronics Specialists Conf., PESC2008, pp. 3986-3991, Rhodes, Greece, 15-19 June 2008.

[6] S. Biricik, S.K. Khadem, S. Redif, M. Basu, "Control of the Dynamic Voltage Restorer to Improve Voltage Quality", IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2014), pp. 1-5, Galway, Ireland, 2014.

[7] S.N. Tackie, E. Babaei, "Modified Topology for Three-Phase Multilevel Inverters Based on a Developed H-Bridge Inverter", Electronics, Vol. 9, p. 1848, 2020.

[8] I.Y. Chung, S.Y. Park, S.I. Moon, I.I. Seong, S.I. Hur, "The control and analysis of zero sequence components in a DVR system", IEEE Proc. of PES Winter Meeting, 2000.

[9] C. Zhan, A. Arulampalam N. Jenkins, "Four-wire dynamic voltage restorer based on a three-dimensional voltage space vector PWM algorithm", IEEE Trans. on Power Electron., vol. 18, no. 4, pp. 1093-1102, July 2003.

[10] C. Zhan, V.K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, S. Kromlidis, M. Barnes, N. Jenkins, "Dynamic voltage restorer based on voltage-space-vector PWM control", IEEE Trans. on Ind. Applicat., vol. 37, no. 6, pp. 1855-1863, Nov./Dec. 2001.

[11] J. Nielsen, M. Newman, H. Nielsen, F. Blaabjerg, "Control and testing of a dynamic voltage restorer at medium voltage level", IEEE Trans. on Power Electron., vol. 19, no. 3, pp. 806-813, May 2004.

[12] H. Kim, S.K. Sul, "Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme", IEEE Trans. on Power Electron., vol. 20, no. 5, pp. 1169-1177, Sept. 2005.

[13] A. Ghosh, A.K. Jindal, "Design of a capacitor supported dynamic voltage restorer for unbalanced and distorted loads", IEEE Trans. on Power Delivery, vol. 19, no. 1, pp. 417-422, Jan. 2004.

[14] Y.W. Li, F. Blaabjerg, D.M. Vilathgamuwa, P.C. Loh, "Design and comparison of high performance stationary-frame controllers for DVR implementation", IEEE Trans. Power Electron., vol. 22, no. 2, pp. 602-612, March 2007.

[15] P. Verdelho, G.D. Marques, "Four-wire current-regulated PWM voltage converter", IEEE Trans. on Ind. Electron., vol. 45, no. 5, pp. 761-770, Oct. 1998.

[16] E. Babaei, M. F. Kangarlu, M. Sabahi, "Mitigation of Voltage Disturbances Using Dynamic Voltage Restorer Based on Direct Converters", IEEE Transactions on Power Delivery, vol. 25, no. 4, October 2010.

[17] J. Matas, M. Castilla, L.G. de Vicuna, J. Miret, J.C. Vasquez, "Virtual impedance loop for droop-controlled single-phase parallel converters using a second-order general-integrator scheme", IEEE Transactions on Power Electronics, vol. 25, no. 12, pp. 2993-3002, January 2011.

[18] P. Rodriguez, A. Luna, R.S. Munoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu, F. Blaabjerg, "A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions", IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 99-112, 2012.

[19] A. Kulkarni, V. John, "A Novel Design Method for SOGIPLL for Minimum Settling Time and Low Unit

Vector Distortion", The 39th Annual Conference of the IEEE in Industrial Electronics Society (IECON 2013), pp. 274-279, Vienna, Austria, 10-13 November 2013.

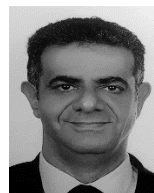
BIOGRAPHIES



Samet Biricik was born in Nicosia, Cyprus in 1984. He received the B.Sc., M.Sc. and Ph.D. degrees in Electrical and Electronic Engineering from Near East University, Nicosia, Northern Cyprus in 2006, 2009 and 2013, respectively. His teaching activities and research interests include power quality, active power filters, electrical machine design, and power electronics. He was assigned Assist. Prof. in 2014 and Assoc. Prof. in 2020. He is also serving as a researcher at Technological University of Dublin, Dublin, Ireland. He was a founder member of the Energy Professionals Association (EPA) and a member of IEEE and Cyprus Turkish Chamber of Electrical Engineers, Northern Cyprus. He is also managing director of Biricik Electrical Engineering Ltd., Northern Cyprus. He is working on the design and manufacturing of reactive power compensators, voltage regulators, asynchronous motor starters and transformers.



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