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DESIGN OF AN AREA AND POWER EFFICIENT MODIFIED CMOS RING OSCILLATOR

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Abstract- In today's world clock, signals play a significant role in different applications, such as communication systems, data acquisition systems, timing generators, global positioning systems, and IOT systems. Ring oscillators (ROs) are used to generate clock signals. Due to the shrinking of technology, demand for low-power RO with smaller chips is increasing manifold. To address both issues, in this manuscript, an inverter circuit having a higher propagation delay has been conceptualized which can be used to design RO for the generation of clock signal. The proposed inverter consists of two cascaded stages: the inverted inverter and the current-starved inverter. The proposed RO is designed to generate a 10 MHz clock signal in Cadence Virtuoso using 180 nm technology. The total power consumption of the designed RO is 234.48 µW. There is a reduction of 22 transistors in this design for the same oscillation frequency.

Keywords: Modified Inverter, Current Starved Inverter, CMOS, Average Power.

1. INTRODUCTION

Inverters and ring oscillators (ROs) are indispensable for the design of different CMOS VLSI applications such as random number generators, switched capacitor circuits, low power clocking, programmable operational amplifiers, and nonoverlapping clock (NOC) [1-4]. The demand for low-power and miniature ROs is increasing rapidly due to technology scaling. The ROs can be designed in different ways. The simplest way to design ROs is by keeping an odd number of closed-loop series inverters or delay blocks. The oscillation frequency of RO is inversely proportional to the propagation delay of each inverter. Each inverter's propagation delay must be increased to generate a low oscillation frequency. In [5], RO is presented using modified CMOS inverters. The reported inverter in [5] consists of two series blocks. First, a CMOS inverter is utilized, followed by an inverted inverter. The output at the end is reduced by threshold voltage on both sides, which causes the propagation delay to increase substantially.

However, the RO presented here suffers from a logic restoration problem. In [6], RO is reported to improve the propagation delay of each inverter further by applying truncated supply voltage to different inverters. Here, different supply voltages are considered for different inverters. The low-frequency RO and NOC design is reported [7] using a modified inverter with enhanced delay. The modified inverter combines voltage scaled CMOS inverters and transmission gates. The reported RO is designed by cascading a CMOS inverter with reduced supply voltage and a transmission gate. In [8], RO is presented by the varying delay of each inverter stage by varying the supply current. In [9], RO is reported for low-power operation by altering the second block of [5].

In this instance, an inverted current-starved inverter takes the role of the second block. An RO is reported for the IOT application in [10] using a modified current-starved inverter. To generate low-frequency oscillation, the delay of each inverter is required to increase further. Many recent CMOS oscillators are reported from [11-17] for different applications. In this work, a small-die area-based inverter with low power consumption named as modified inverted current starved inverter with current starved inverter (MICSICSI) is proposed to design an RO. The operation details of the proposed inverter and RO concepts are discussed in the next Section. The results are presented and discussed in Section 3. In the next Section, a conclusion is drawn from the work.

2. PROPOSED INVERTER MICSICSI

The proposed configuration of the inverter "MICSICSI" is shown in Figure 1. The MICSICSI is comprised of two stages. In the first stage, a modified inverted current starved inverter is considered consisting of three NMOS and three PMOS transistors. One PMOS and one NMOS transistor are added in the top and bottom of the first stage of [10]. In the next stage, a current-starved inverter (CSI), consisting of two NMOS and two PMOS transistors, is considered. The operation of the proposed inverter is divided into parts. First, MICSICSI behaves as a cascaded pass transistor [18].

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Due to the addition of both transistors, a reduction in current flowing through the first stage occurs. After the first stage, the output is reduced by approximately one threshold voltage from both ends (V_{DD}, V_{TP}, V_{TN}). Secondly, the same output is fed to the CSI as an input. The CSI behaves as a normal inverter capable of restoring the previous stage output.

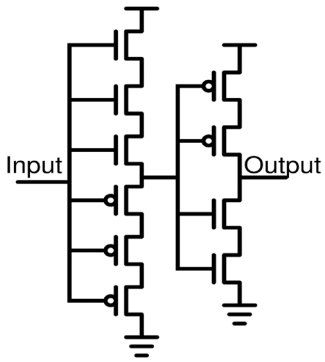

Figure 1. Proposed structure of MICSICSI

2.1. MICSICSI-Based Ring Oscillator

The CMOS ROs are extensively used in various applications due to their simplicity of design and analysis. For this category of CMOS RO, an odd number of inverter connections is accomplished successively in a closed-loop configuration. The RO oscillates at a particular frequency when the phase shift of RO is exactly 2π with a unity close loop gain. Many tradeoffs exist in the design of the RO, such as power, area, phase noise, figure of merit, etc. [1]. The oscillation frequency (f_{osc}) of RO is represented as [5]:

$$f_{osc} = \frac{1}{2m\tau} \quad (1)$$

where, m represents the number of inverters connected in RO, and the propagation delay of the inverter is represented by τ. In this work, RO is designed with MICSICSI, which provides a higher delay than other traditional inverters for the generation of lower oscillation frequency. The configuration of MICSICSI RO is depicted in Figure 2.

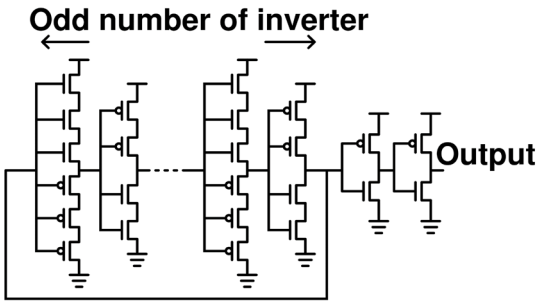

Figure 2. MICSICSI-based ring oscillator

The output of MICSICSI-based RO has both higher fall and rise times because of the availability of limited current for charging and discharging in both stages of the inverter. Hence, buffers are used in the end to get sharper fall and rise time.

3. SIMULATION RESULTS

The design of the proposed RO using five stages of MICSICSI is done in Cadence Virtuoso using GPDK 180 nm technology with a 1.8 Volt supply voltage. The minimum size of NMOS and PMOS transistors is used in MICSICSI design.

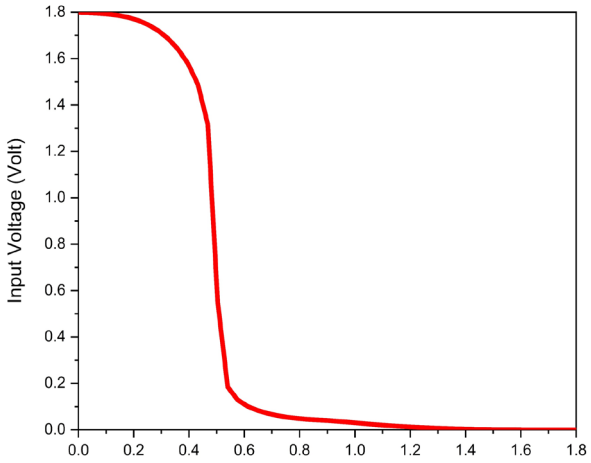

Figure 3. Input vs. output voltage of MICSICSI

Figure 3 depicts the output voltage of MICSICSI due to a change in input voltage. When rail-to-rail voltage is applied at the input of the first stage of MICSICSI, the output swings from 0.33 V to 1.58 V. The upper (lower) voltage, which can be considered as logic 0 (1) by the second stage of MICSICSI, is 0.56 V (0.8 V). So, the second stage of MICSICSI considers the output of the first stage to be perfect "logic 0" and "logic 1". The input and output signals after the first and second stages of the MICSICSI are shown in Figure 4. The transient response of the five-stage MICSICSI-based RO is depicted in Figure 5. The output response of the proposed RO with additional buffers is perfect rail-to-rail from 0 to 1.8 V with a 10.47 MHz oscillation frequency.

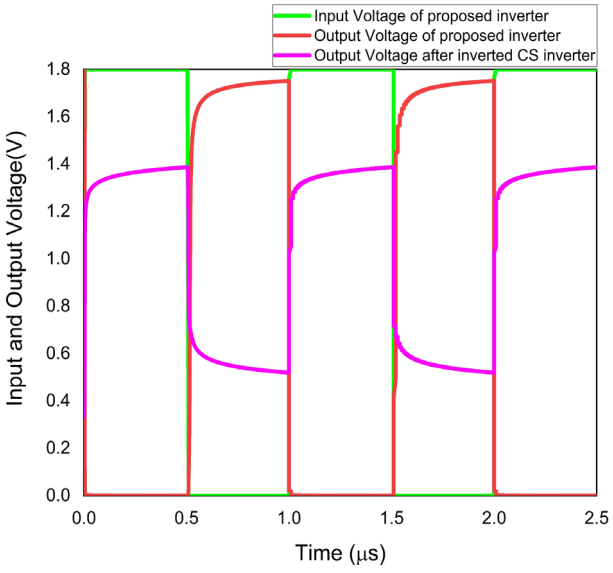

Figure 4. Input and output voltage level of MICSICSI

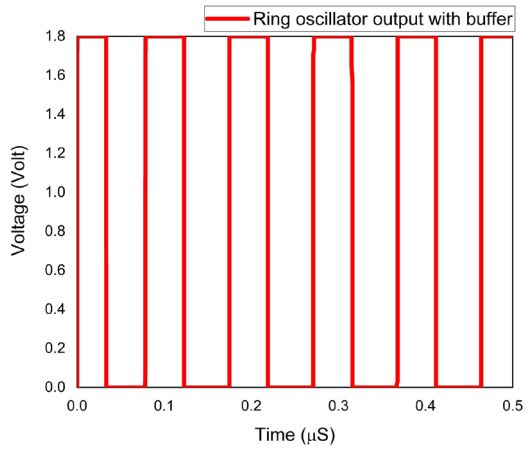

Figure 5. Transient response of RO using MICSICSI

The proposed oscillators process, voltage, and temperature (PVT) analysis is carried out to check the design efficacy. The variation in frequency of oscillation of the MICSICSI oscillator due to a change in supply voltage is depicted in Figure 6. The oscillation frequency varies from 8.45 MHz to 12.5 MHz due to a 10 percent change in supply voltage.

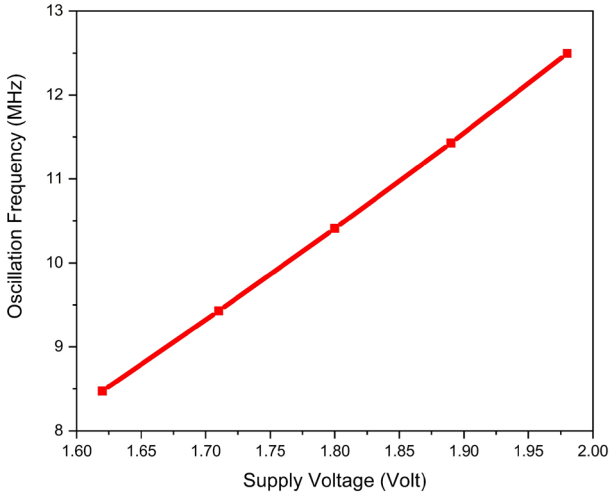

Figure 6. Supply voltage variation analysis of MICSICSI RO

The effect of temperature variation on the proposed RO is shown in Figure 7. The oscillation frequency of the proposed oscillator varies from 3.4 MHz to 24.08 MHz due to changes in temperature from –40 °C to 125 °C. The effect of process variation on the proposed RO is shown in Figure 8. It is evident from Figure 8 that the variations from Nominal-Nominal (NN) to Slow-Slow (SS) and Fast-Fast (FF) processes are less as compared to Slow-Fast (SF) and Fast-Slow (FS) processes. From the PVT analysis of the proposed RO, it is evident that RO performance is not affected compared to its counterpart design. The performance parameters such as the transistor area, DC power, average power, and oscillation frequency of the proposed RO are compared with [10] and presented in the Table 1. The MICSICSI-based RO is designed with five inverter stages for comparison with the oscillator reported in [10].

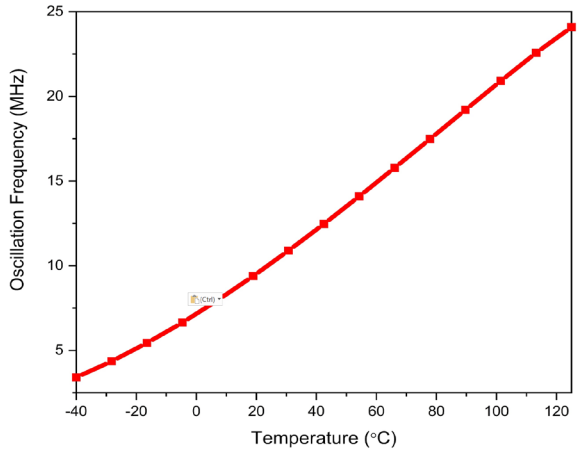

Figure 7. Temperature variation analysis of MICSICSI RO

The frequency of oscillation of the MICSICSI oscillator is improved to 10.47 MHz as compared to 17.56 MHz for approximately the same power consumption. To generate the same frequency of oscillation using RO [10], 76 transistors are required due to which power consumption will also be increased. Table 1 establishes the area and power effectiveness of the proposed MICSICSI RO. The size of all transistors can be optimized further using different optimization technique [19-20] to improve the propagation delay.

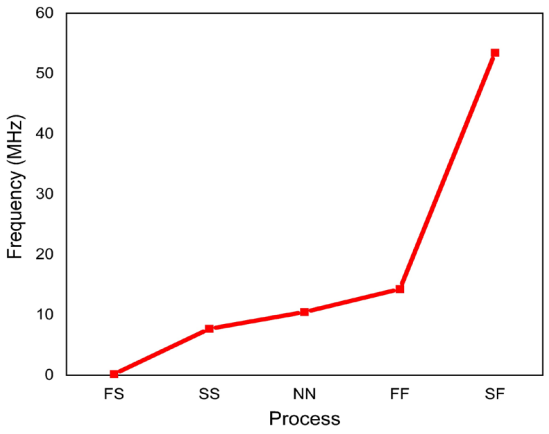

Figure 8. Process variation analysis of MICSICSI RO

Table 1. Comparison of performance parameters

Performance Parameters	RO [6]	RO [7]	RO [10]	Proposed work
Technology used (nm)	180	180	180	180
Supply voltage (V)	1.8	1.8	1.8	1.8
Frequency (MHz)	325	150	17.56	10.47
Number of inverter stage	25	27	5	5
Transistors count	50	110	44	54
DC power (µW)	NR	NR	144.7	144.36
Average power (µW)	53.12	960	84.85	90.12

6. CONCLUSION

In this work, a novel inverter (MICSICSI) is proposed to generate a higher propagation delay. The MICSICSI is used to design a low power and area efficient ring oscillator. The simulation results show that a five-stage MICSICSI RO has a 10.47 MHz oscillation frequency with 144.36 µW power dissipation.

The process, voltage and temperature variation results show oscillation frequency variations lies within the required range. The simulation results establish the effectiveness of the MICSICSI based RO. The proposed RO is a good choice for area and power-efficient low-frequency clock generation. The MICSICSI based can be explored further to design non-overlapping clock (NOC) for switched capacitor circuits. The supply voltage scaling of MICSICSI can be explored further for improvement in propagation delay. The width and length of each transistor can be optimized further to get the better results. Next work will be focused on the implementation and testing of MICSICSI

NOMENCLATURES

1. Acronyms

RO	Ring Oscillator
MICSICSI	Modified Inverted Current Starved Inverter with Current Starved Inverter
PVT	Process, Voltage, Temperature
VLSI	Very Large-Scale Integration

2. Symbols / Parameters

m: Number of inverter stages
τ: Propagation delay of inverter
f_{osc}: Oscillation frequency

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