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ENHANCED SINGLE-PHASE H-BRIDGE MULTILEVEL INVERTER FOR EFFICIENT RENEWABLE ENERGY CONVERSION

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Abstract- This study presents an enhanced single-phase H-bridge multilevel inverter for efficient renewable energy conversion. Symmetric and asymmetric analysis of the topology is presented. The proposed inverter uses 12 semiconductor switches, 12 drivers, and 6 DC sources. The symmetric configuration of the proposed topology generates nine voltage levels, while the asymmetric one generates 31 voltage levels, a higher voltage level is more suitable for renewable energy applications such as solar energy. This is due to the output waveforms containing fewer distortions. The topology utilizes fewer components to produce a sinusoidal high-level and high-quality waveform, increasing the inverter's efficiency and reducing the cost. A fundamental frequency control technique is used because it is simpler to implement and reduces switching losses. A comparative evaluation of the presented topology's components to conventional multilevel inverters and other published topologies is illustrated. PSCAD/EMTDC is used for the investigation and simulation of the presented single-phase multilevel inverter. Simulation outcomes support the theoretical calculations of standing voltages and the performance of the proposed topology.

Keywords: Multilevel Inverter, Single-Phase H-bridge Inverter, Renewable Energy Sources.

1. INTRODUCTION

In recent years, the use of power electronic converters has grown significantly, making them a necessary component for the conversion of electrical energy across all power classes. Recent developments in the world of technology have made renewable energy systems increasingly viable options, making multilevel inverter an intriguing field of study. Multilevel inverters, in contrast to two-level inverters, create a higher number of voltage levels that are mostly used in medium-voltage, high-power applications [1-4]. A multilevel inverter (MLI) generates a staircase waveform at the output using one or several DC voltage sources

MLI offers a lot of advantages over traditional two-level inverters. These include lowering the amount of stress placed on semiconductor devices, decreasing electromagnetic interference, lowering total harmonic distortion (THD), scaling up the process, increasing the output voltage levels, using lower-rated switches, producing high-quality output waveforms, and reducing the size and volume [5-7]. An inverter's limitations include its inability to run at high voltages, increased power quality problems, and extreme switching voltage stress. Additionally, these issues contribute to the very low efficiency of renewable energy systems. As a result, multilevel inverters are crucial for renewable energy applications as they help solve issues related to conventional inverters [8-9].

Three fundamental topologies for conventional multilevel inverters have been defined as the flying capacitor MLI, the clamping diode (Neutral point clamped) MLI, and the cascaded H-bridge MLI [10-13]. The most commonly used MLI is the CHB MLI because of its simplicity of operation and potential, which elevates this type of inverter to attention. For the majority of the time, industrial applications use cascaded H-bridge MLI to integrate renewable energy [14-17]. This MLI topology does not necessarily need voltage balancing capacitors or voltage clamping diodes, in contrast to the FC and DC MLI designs. The cascaded structures are categorized into two parts, known as symmetric and asymmetric MLI. For symmetric structures, the magnitudes of all input DC voltage sources are the same. While for the asymmetric structure, the magnitudes are different. The advantage of an asymmetric structure is that it's able to produce higher output voltage steps while utilizing the exact amount of components in a symmetric structure. Constructing an asymmetric multilevel inverter takes less area and costs compared to a symmetric with the same output levels [18-19]. Modern research in multilevel inverters aims to improve topological structures and control strategies [20-24]. Step output voltages must be increased while reducing the number of components in any improved MLI system to advance the effectiveness of the newer topologies.

An asymmetric 17-level MLI topology is proposed in [25], which optimizes the number of power components, resulting in a smaller and more efficient system. The study

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reports a current THD of 2.36%, reflecting the inverter's effectiveness in delivering high-quality power for grid applications. Further investigation is needed to explore scalability limitations and assess the inverter's behavior under different load scenarios. Also, [26] proposed a DSTATCOM-based 9-level multilevel inverter that utilizes additive and subtractive configurations to achieve higher output levels. Compared to earlier topologies, this approach significantly reduces the number of active switches required and lowers the THD.

This study [27] presents the Imperialistic Competitive Algorithm (ICA) as a method to solve the SHE problem in Cascaded Multilevel Inverters (CMLI) with equal DC sources. This method significantly improves the determination of optimal switching angles and reduces computational demands. The method's effectiveness is validated through simulation and experimental results on an 11-level cascaded H-bridge inverter.

With its better waveform quality and reduced component requirements, the proposed inverter is well-suited for diverse applications, such as power quality management and integration into smart grid systems. With an emphasis on achieving stable and efficient power distribution, the proposed inverter is well-suited to minimize losses and harmonic distortions as well as improve voltage levels across various engineering applications.

The proposed topology achieves a 31-level output with fewer semiconductor switches and DC sources, a significant improvement over conventional single-phase H-bridge and other multilevel topologies. This design differentiates itself from earlier works that require complex arrangements or additional components, like clamping diodes and capacitors, by optimizing efficiency and waveform quality with an asymmetric configuration, as shown in [reference]. Through a comparative analysis, this study reveals that the proposed topology reduces the overall component count and enhances the quality of the output waveform, positioning it as an ideal choice for renewable energy conversion.

The content of this paper introduces an enhanced single-phase H-bridge multilevel inverter for efficient renewable energy conversion that has fewer drives, switches, and DC sources and generates increased levels of output voltage with more efficiency and quality sinusoidal waveforms.

The other sections of the paper are arranged as follows: section 2 details the proposed single-phase H-bridge topology and symmetric and asymmetric analysis of the topology. In section 3, the fundamental frequency control method is explained. Section 4 shows the juxtaposition study of the presented topology to other existing topologies, comparing the number of components used. In section 5, the power loss calculation is presented, as well as the standing voltage. Section 6 provides the results of the simulation. Section 7 provides conclusion.

2. PROPOSED TOPOLOGY

The proposed topology is depicted in Figure 1. The topology utilizes fewer components to generate step voltage levels for renewable energy conversion. The components required are 6 DC voltage sources, 12 power switches, and their respective driver circuits. The load of the topology is a resistance-inductance (RL) load. The employed DC voltage sources are isolated ones to guarantee safe operation and reliable voltage level generation that is produced by renewable energy sources, for example, PV, wind, fuel cells, etc. The switches used are bidirectional and unidirectional from a voltage point of view. IGBT switches are preferred over MOSFETs for their lower conduction losses in high-power applications, ensuring efficient operation of the 31-level output and effective thermal management. The switches S_5, S_6, S_{11}, and S_{12} are bidirectional, and other switches are unidirectional. The unidirectional switches are made of one diode and IGBT, which blocks voltage in one direction, while the bidirectional consist of two antiparallel diodes and two IGBTs, which block voltage in both directions. The common emitter technique is used to reduce the number of drivers. Furthermore, if there is an open circuit of the inductive load or a short circuit for the sources, there will be no output parameters, these are considerations to be avoided. For example, the power switches of (S_1, S_2), (S_3, S_4), and (S_5, S_7) must not be activated simultaneously to avoid short circuits of the sources.

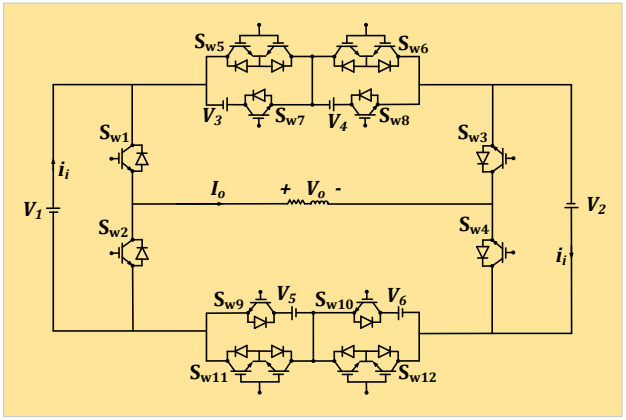


Figure 1. Proposed topology

$$\begin{cases} N_{Sources} = 6 \\ N_{Switches} = 12 \\ N_{Driver} = 12 \\ V_3 = V_5 \\ V_4 = V_6 \end{cases} \quad (1)$$

Equation (1) states the components of the topology, the number of DC sources, which are 6, and the voltage source V_3 is equal to V_5 in terms of magnitude and the same for V_4 and V_6. The topology can generate both positive and negative output voltage levels as it uses an H-bridge structure. In the topological structure, there are 2 DC voltage sources on the upper section, V_3 and V_4, and 2 on the lower section, V_5 and V_6. These 4 DC sources, 1 from the upper and 1 from the lower section, have equal voltage magnitudes and the same for the other two DC sources to achieve the same value of positive and negative steps.

The dc sources are arranged in series to raise the load voltage steps. Symmetric and asymmetric DC voltage sources yield diverse output voltage steps. Symmetric topology produces nine voltage levels, while asymmetric generates a maximum of 31 output voltage levels, 15 positive levels, 0V level, and 15 negative levels.

By employing an asymmetric DC source arrangement, the proposed inverter introduces a novel approach that allows it to produce a 31-level output using only 12 power switches, whereas traditional topologies require more components to achieve the same voltage levels. By minimizing components, the design enhances efficiency, making it an ideal solution for renewable applications where both cost and the reliability of components are crucial.

2.1. Symmetric DC Sources

Symmetric magnitudes mean the DC sources will have an equal magnitude of voltage. Symmetric topology produces nine voltage levels. The upper section of the proposed topology will not be activated (open) when producing the positive voltage levels, and the same for the bottom structure when generating negative levels. The related input DC source magnitudes and maximum output voltage for symmetric structure are shown in Equation (2), where input voltage $V_{in,dc}$ is the same magnitude for every voltage source, the maximum output voltage is expressed as well stating the voltage levels and adding together:

$$\begin{cases} V = V_{in,dc} \\ V_1 = V_2 = V_3 = V_4 = V_5 = V_6 \\ V_{o,\max} = V_1 + V_2 + V_5 + V_6 = 4V_{in,dc} \end{cases} \quad (2)$$

The switching states for the symmetric case are shown in Table 1. Some switching operations of the inverter shown in Figure 2 display the current path and the switches gated on to produce a certain number of voltage levels. Furthermore, in symmetric operations, there are many combinations of switches turned on for most cases to generate equivalent output voltage levels; few are used in the table, and the switching states figure to get the idea. For example, there are four paths to generate $1V_{in,dc}$, which activates any one of the four dc sources.

Table 1. Switching Pattern for Symmetric Sources

Modes	Switches ON	V_o
I	S_1, S_3, S_9, S_{10}	$4V_{in,dc}$
II	S_1, S_3, S_{10}, S_{11}	$3V_{in,dc}$
III	S_1, S_3, S_{11}, S_{12}	$2V_{in,dc}$
IV	S_1, S_4, S_{11}, S_{12}	$1V_{in,dc}$
V	S_2, S_4, S_{11}, S_{12}	0
	S_1, S_3, S_5, S_6	0
VI	S_2, S_3, S_5, S_6	$-1V_{in,dc}$
VII	S_2, S_4, S_5, S_6	$-2V_{in,dc}$
VIII	S_2, S_4, S_5, S_8	$-3V_{in,dc}$
IX	S_2, S_4, S_7, S_8	$-4V_{in,dc}$

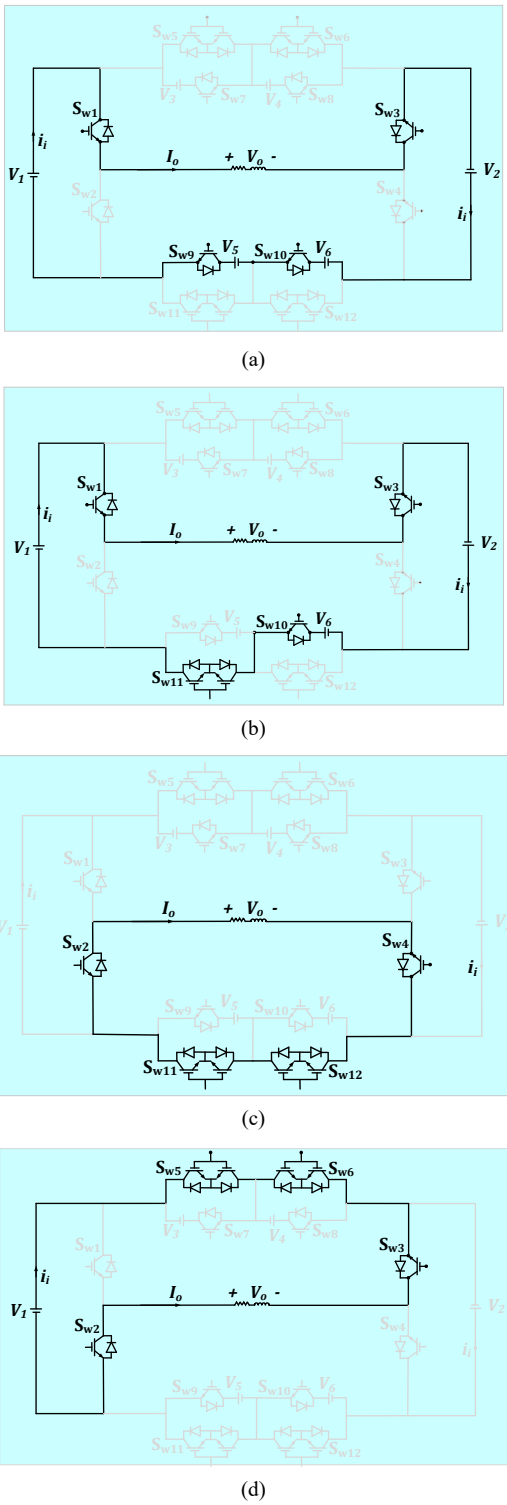


Figure 2. Switching States for Symmetric structure, a) $4V_{in,dc}$, b) $3V_{in,dc}$, c) 0V, d) $-1V_{in,dc}$

2.2. Proposed Asymmetric Single-Phase H-bridge MLI

The asymmetric feature, using different magnitudes of the voltage source, gives higher levels. It will be able to generate a maximum of 31 voltage levels. Comparatively, it's a leap jumped from the symmetric one with nine levels only. Table 2 illustrates the switching pattern for the presented asymmetric topology. The number of step levels N_{Level}, the relations for the DC sources' magnitudes, and

the maximum output voltage, $V_{o,\max}$ are expressed in Equation (3), this details the increase of voltage levels in contrast to the symmetric configuration:

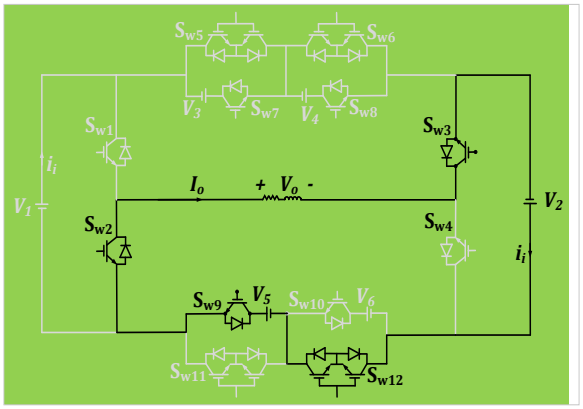
$$\begin{cases} N_{Level} = 31 \\ V_1 = 1V_{in,dc} \\ V_2 = 2V_{in,dc} \\ V_3 = V_5 = 4V_{in,dc} \\ V_4 = V_6 = 8V_{in,dc} \\ V_{o,\max} = V_1 + V_2 + V_5 + V_6 = 15V_{in,dc} \end{cases} \quad (3)$$

Selected switching states shown in Table 2 for the presented topology are shown in Figure 3. The generated voltage levels are both positive and negative values, a total of 31 levels.

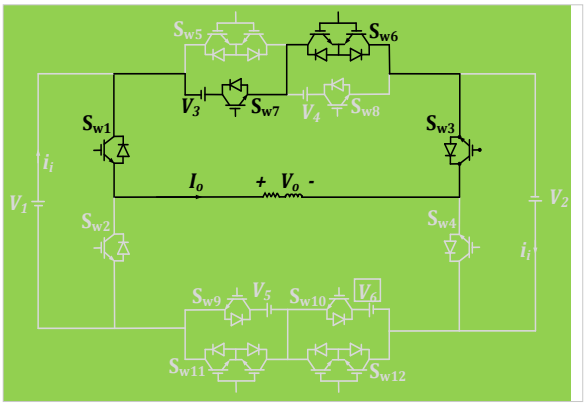
Table 2. Switching Pattern for Symmetric Sources

Mode	Switches ON	Voltages Sources	$V_{o,dc}$
1	S_1, S_3, S_9, S_{10}	$V_1+V_2+V_5+V_6$	$15V_{in}$
2	S_2, S_3, S_9, S_{10}	$V_2+V_5+V_6$	$14V_{in}$
3	S_1, S_4, S_9, S_{10}	$V_1+V_5+V_6$	$13V_{in}$
4	S_2, S_4, S_9, S_{10}	V_5+V_6	$12V_{in}$
5	S_1, S_3, S_{10}, S_{11}	$V_1+V_2+V_6$	$11V_{in}$
6	S_2, S_3, S_{10}, S_{11}	V_2+V_6	$10V_{in}$
7	S_1, S_4, S_{10}, S_{11}	V_1+V_6	$9V_{in}$
8	S_2, S_4, S_{10}, S_{11}	V_6	$8V_{in}$
9	S_1, S_3, S_9, S_{12}	$V_1+V_2+V_5$	$7V_{in}$
10	S_2, S_3, S_9, S_{12}	V_2+V_5	$6V_{in}$
11	S_1, S_4, S_9, S_{12}	V_1+V_5	$5V_{in}$
12	S_2, S_4, S_9, S_{12}	V_5	$4V_{in}$
13	S_1, S_3, S_{11}, S_{12}	V_1+V_2	$3V_{in}$
14	S_2, S_3, S_{11}, S_{12}	V_2	$2V_{in}$
15	S_1, S_4, S_{11}, S_{12}	V_1	$1V_{in}$
16	S_2, S_4, S_{11}, S_{12}	-	0
16	S_1, S_3, S_5, S_6	-	0
17	S_2, S_3, S_5, S_6	$-V_1$	$-1V_{in}$
18	S_1, S_4, S_5, S_6	$-V_2$	$-2V_{in}$
19	S_2, S_4, S_5, S_6	$-(V_1+V_2)$	$-3V_{in}$
20	S_1, S_3, S_6, S_7	$-V_3$	$-4V_{in}$
21	S_2, S_3, S_6, S_7	$-(V_1+V_3)$	$-5V_{in}$
22	S_1, S_4, S_6, S_7	$-(V_2+V_3)$	$-6V_{in}$
23	S_2, S_4, S_6, S_7	$-(V_1+V_2+V_3)$	$-7V_{in}$
24	S_1, S_3, S_5, S_8	$-V_4$	$-8V_{in}$
25	S_2, S_3, S_5, S_8	$-(V_1+V_4)$	$-9V_{in}$
26	S_1, S_4, S_5, S_8	$-(V_2+V_4)$	$-10V_{in}$
27	S_2, S_4, S_5, S_8	$-(V_1+V_2+V_4)$	$-11V_{in}$
28	S_1, S_3, S_7, S_8	$-(V_3+V_4)$	$-12V_{in}$
29	S_2, S_3, S_7, S_8	$-(V_1+V_3+V_4)$	$-13V_{in}$
30	S_1, S_4, S_7, S_8	$-(V_2+V_3+V_4)$	$-14V_{in}$
31	S_2, S_4, S_7, S_8	$-(V_1+V_2+V_3+V_4)$	$-15V_{in}$

The 0V mode has two states, either S_1, S_3, S_5, and S_6 or S_2, S_4, S_{11}, and S_{12} are turned on separately. To produce 15 positive levels ($V_{in,dc}$), the switches S_1, S_3, S_9, and S_{10} are gated on all at once. The conduction in each state produces a one voltage level, while one state is conducting, the other states have to be in blocking mode. To generate levels in the order from the highest to the lowest output voltage, the path for the switching has to depend on the sources we gate on following Figure 3. The positive voltage level of 14 is generated when S_2, S_3, S_9, and S_{10} are switched on, and 13 positive level is when these switches, S_1, S_4, S_9, and S_{10} are switched on. To generate positive 10 output levels, the sources V_6 and V_2 generate 10 levels, therefore, switches S_2, S_3, S_{10}, and S_{11} are gated on.



(a)



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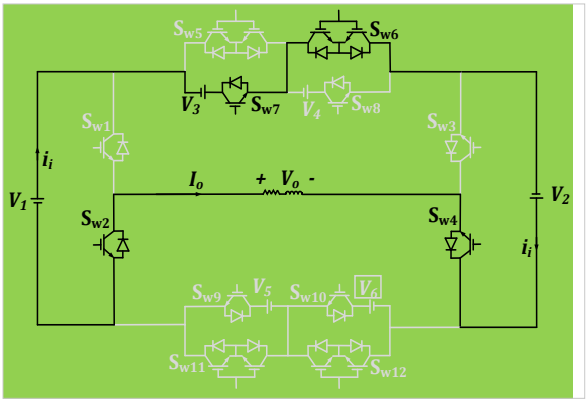

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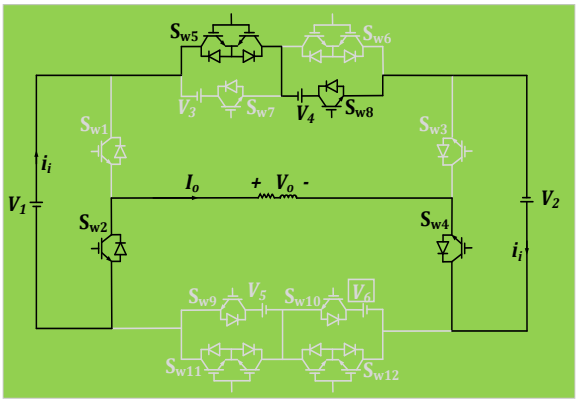

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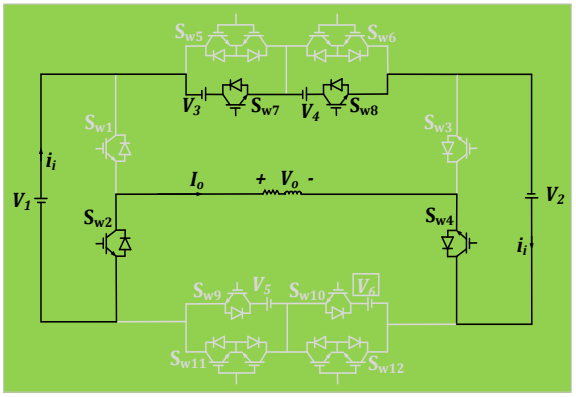


(e)

Figure 3. Switching States for Asymmetric Proposed Topology, a) $6V_{dc}$, b) $-4V_{dc}$, c) $-7V_{dc}$, d) $-9V_{dc}$, e) $-15V_{dc}$

3. FUNDAMENTAL FREQUENCY CONTROL

The control technique used to control the improved single-phase H-bridge inverter presented is the fundamental frequency control method (FFCM), it is simpler and more efficient than some other control methods. It is also called nearest level control (NLC). It picks the voltage level the multilevel inverter will produce, uses the reference load voltage waveform and the staircase voltage levels, and chooses the nearest level. It is illustrated in Figure 4. The steps of the voltage levels determine the normalization of the waveform of the reference voltage, the value taken is the closest integer. The product of the integer and voltage source magnitude gives the voltage level the inverter generates. Among its benefits is if more phases are initiated, it will control every phase separately and shift an angle difference of 120°.

This topology incorporates fundamental frequency control to strategically improve efficiency, making it well-suited for renewable energy sources. Compared to more elaborate control methods, FFCM enhances energy efficiency by reducing switching losses by selecting the nearest level according to the reference waveform. This control strategy, paired with the asymmetric configuration, positions the inverter as reliable with a high-quality output waveform and energy-efficient solution for renewable energy conversion.

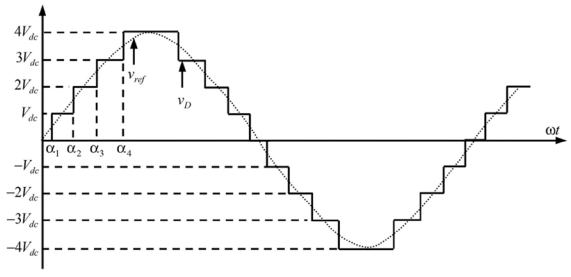


Figure 4. Fundamental frequency control method

The system flow diagram in Figure 5 details the sequence, designing the circuit, and selecting DC sources 12-switches. Using fundamental frequency control, implementing gate signals for specific voltage levels, and analyzing load results.

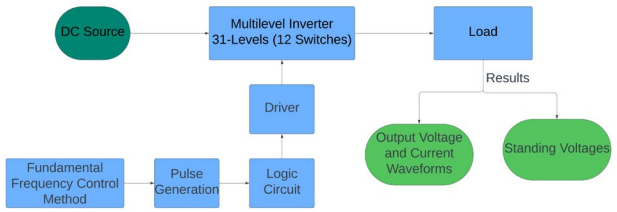


Figure 5. Flowchart of the system

4. POWER LOSSES

Inverter's power losses happen in the switches during the on and off states. There are three power losses of the switches, and the summation of those are the total losses of the inverter. The three power losses are:

1. Switching losses
2. Blocking losses
3. Conduction losses

The graph in Figure 6 shows the power losses and the period in which each occurs. The blocking losses are not considered, and it's negligible. It has low power loss because the current during off-mode is lower.

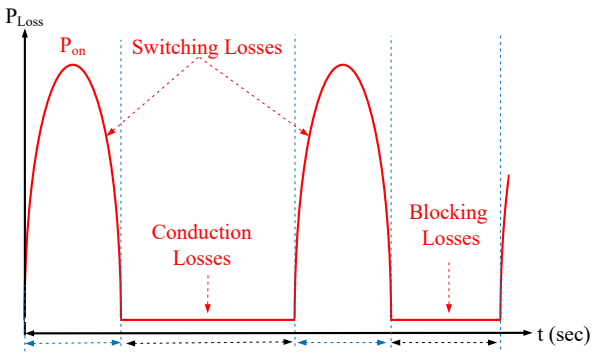


Figure 6. Inverter power losses

4.1. Switching Losses

These losses happen in on and off states. It is dependent on time as shown in the graph of Figure 5. The summation of the switching losses in on-mode and off-mode is the total losses of the switching. Switching losses are determined by considering the on-state and off-state switching intervals of each IGBT switch, calculated as by Equations (4)-(6):

$$\begin{cases} E_{on} = \int_0^{t_{on}} v(t)i(t)dt \\ E_{on} = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}}t\right)\left(-\frac{V_{sw}}{t_{on}}\left(t-t_{on}\right)\right)\right]dt \\ E_{on} = \frac{1}{6}V_{sw}I't_{on} \end{cases} \quad (4)$$

$$\begin{cases} E_{off} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw}It_{on} \\ E_{off} = \int_0^{t_{off}} \left[\left(\frac{V_{sw}}{t_{off}}t\right)\left(-\frac{I}{t_{off}}\left(t-t_{off}\right)\right)\right]dt \\ E_{on} = \frac{1}{6}V_{sw}It_{off} \end{cases} \quad (5)$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left[\sum_{i-1}^{N_{on}} E_{on} + \sum_{i-1}^{N_{off}} E_{off} \right] \quad (6)$$

where, E_{on} is the switching losses during the on state, which is a sixth of the product of voltage in the off state, current during the off state, and period time. Similar to the E_{off} in off state, hence the P_{SW} is the total switching losses, which is the summation of E_{on} and E_{off} multiplied by the switching frequency f_s.

4.2. Conduction Losses

Conduction losses happen during the on-mode. Semiconductor power switches of the presented topology consist of unidirectional and bidirectional switches, which are made of IGBTs and diodes. P_C is expressed as the total conduction losses. In the on-mode, the power losses of the IGBT and the diode are summed to get the total conduction power losses. $P_{C,T}$ is expressed as the conduction loss for the transistor, and $P_{C,D}$ is for the diode. V_T and V_D are the voltage components of the transistor and diode, and R_T and R_D are the resistive components of the transistor and diode. Equation (7) is the conduction losses of the transistor, $P_{C,T}$. Equation (8) is the conduction losses for the diode, $P_{C,D}$. Equation (9) is the total losses, P_C given by adding both equations.

$$\begin{cases} P_{C,T}(t) = \left[V_T + R_T i^{\beta}(t) \right] i(t) \\ P_{C,T}(t) = \dfrac{1}{2\pi} \displaystyle\int_0^{2\pi} n_T \left[V_T + R_T i^{\beta}(t) i(t) \right] d(\omega t) \end{cases} \quad (7)$$

$$\begin{cases} P_{C,D}(t) = \left[V_D + R_D i(t) \right] i(t) \\ P_{C,D} = \dfrac{1}{2\pi} \displaystyle\int_0^{2\pi} n_D(t) \left[V_D + R_D i(t) i(t) \right] d(\omega t) \end{cases} \quad (8)$$

$$P_C = P_{C,T} + P_{C,D} \quad (9)$$

The total losses of the inverter circuit, P_{Losses} is calculated by adding switching losses, conduction losses, and blocking losses. But blocking losses are negligible. Therefore, the total losses and the efficiency are given Equations (10) and (11), accordingly. These equations ensure consistency with standard power electronics models, accurately reflecting the inverter's performance under different operating conditions.

$$P_{Losses} = P_{SW} + P_C \quad (10)$$

$$\eta = \frac{P_{out}}{P_{input}} \quad (11)$$

4.3. Standing Voltage

The standing voltage, also known as the blocking voltage of an inverter, is calculated through the power switches in the circuit when they are not conducting in their off state. When the switch is 'on,' the blocking voltage is zero. The maximum voltage that the switch can handle in its off mode is the blocking voltage of that switch. The summation of all the blocking voltage of the switches gives the blocking voltage of the inverter.

The blocking voltages depend on the voltage sources of the inverter; it is important to choose a switch with lower blocking voltages as higher voltages of power switches cost more. In the proposed MLI, we have 12 power switches; the blocking voltages of the switches are expressed by Equation (12).

$$\begin{cases} V_{S1} = V_{S2} = V_1 = V_{in,dc} \\ V_{S3} = V_{S4} = V_2 = 2V_{in,dc} \\ V_{S5} = V_{S7} = V_{S9} = V_{S11} = V_3 = 4V_{in,dc} \\ V_{S6} = V_{S8} = V_{S10} = V_{S12} = V_4 = 8V_{in,dc} \end{cases} \quad (12)$$

The inverter standing voltage is computed by Equation (13):

$$\begin{cases} V = 2\left(V_{in,dc}\right) + 2\left(2V_{in,dc}\right) + 4\left(4V_{in,dc}\right) + 4\left(8V_{in,dc}\right) \\ V = 54V_{in,dc} \end{cases} \quad (13)$$

5. COMPARISON ANALYSIS

This part compares the proposed topology, the single-phase H-bridge MLI, with other published topology inverters by looking at the number of components in the circuit construction. The topologies compared all have the same levels of voltage levels, which is 31 output voltages. Table 3 shows the comparison of these topologies.

The comparison in Table 3 shows the total components of the proposed topology is 46, including the driver circuits. There are four bidirectional switches, in which the number of IGBT and diodes are higher than the driver circuit, two switches sharing a common emitter, and one circuit driver. The three conventional multilevel inverters have a higher quantity of components, more DC sources for CHB MLI, clamping diodes for NPC MLI, and other clamping capacitors for FC MLI. Some topologies have advantages over the proposed one; the presented inverter has 6 DC sources higher than most topologies except [28]. Topology [31] has the least component count, having 3 DC sources and 2 switches less than the propounded topology. The components of the proposed single-phase H-bridge MLI are among the smallest, therefore reducing the cost, maintenance, and losses of the inverter.

Table 3. Comparison topologies analysis

Topology	Proposed	[28]	[29]	[30]	[31]	[32]	[33]
Voltage Level	31	31	31	31	31	31	31
DC Source	6	15	2	2	3	4	4
Switches	12	18	16	18	12	16	12
Driver	12	18	16	18	10	16	12
Diode	16	32	18	20	12	16	12
Clamped Diode	0	0	0	0	0	0	0
Capacitor	0	0	4	4	4	0	0
Clamped Capacitor	0	0	0	0	0	0	0
All Component	46	83	56	62	38	52	40

While the proposed inverter is efficient and uses fewer components, its practical deployment in renewable applications presents challenges, such as the potentially high costs of IGBT switches and DC sources in larger systems, cost efficiency could be improved by considering alternative materials and simplifying circuit components within the design. Optimized heat sinks and liquid cooling can alleviate thermal concerns and support stable

operation. Lastly, durability is vital for renewable energy systems exposed to fluctuating environments. Incorporating tough, weather-resistant materials enhances the inverter's resilience, allowing it to perform reliably over extended durations.

As shown in Table 4, This inverter topology stands out with a reduced component requirement—just 12 switches and 6 DC sources—cutting costs and simplifying the circuit while maintaining a high 95% efficiency. However, topology [34] has fewer voltage sources but has a few more losses; it is less efficient than the proposed topology. Traditional CHB inverters typically need a larger number of components and involve greater costs, whereas the proposed inverter offers a more efficient and cost-effective solution for renewable energy.

Table 4. Component count and efficiency comparison

Topology	Level	Component Count	Efficiency
Proposed	31	12 switches, 6 DC sources	95.39%
[34]	31	12 switches, 4 DC sources	93.51%
Cascaded H-Bridge (CHB)	31	60 switches, 15 DC sources	~90%

6. SIMULATION RESULTS

The simulation of the proposed topology is done in PSCAD software. The circuit has 12 power switches and 6 DC sources. The load is made of resistance and inductance. 4 switches are bidirectional. Table 5 shows the parameters for the simulation setup.

The parameters in the table show the load frequency is 50Hz, the standard frequency for an AC system, and the switching frequency is 50kHz. When the switching frequency is increased, the higher the switching losses and conduction losses, but the advantage of higher frequency is the better quality of the output waveforms.

Table 5. Simulation parameters

Parameter	Magnitude
Output Frequency (f_0)	50 Hz
Output Resistance (R)	50 Ω
Modulation Index	1
Output Inductance (L)	0.05 H
Switching Frequency (f_s)	50 kHz
Voltage Sources	V_1=22V, V_2=44V, V_3=V_5=88V, V_4=V_6=176V

The simulation of the proposed single-phase H-bridge MLI generated output waveforms of 31 levels. The output voltage steps and the reference voltage waveforms are illustrated in Figure 7. The quality of the output voltage waveform is better because it is in the same pattern as the reference sine wave. The highest produced output voltage is 330V, the peak voltage for standard AC, and each step equates to 22V. Figure 8 depicts the output current waveform of the inverter, the amplitude of the current is 6.35A, and the quality of the waveform is perfect. The blocking voltage of all 12 switches is seen in Figure 9. The standing voltages calculated in theory for the switches are the same as shown in the simulation. Switch S_1 has a standing voltage of 22V, and switch S_2 is also 22V. The waveforms of the standing voltages show the time when the switch is in blocking mode, as seen in the graph, it is opposite for S_1 and S_2, and the same for S_3 and S_4 to avoid short circuits and generate the stepped output voltage levels. S_3 and S_4 have 44V standing voltage. S_7 and S_9 is 88V, S_8 and S_{10} is 176V.

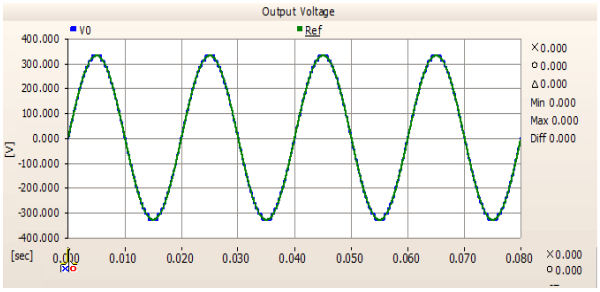


Figure 7. Output voltage and reference waveform

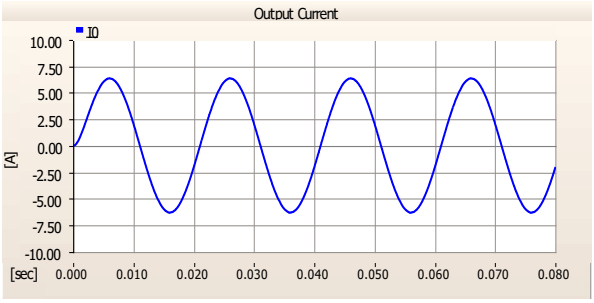
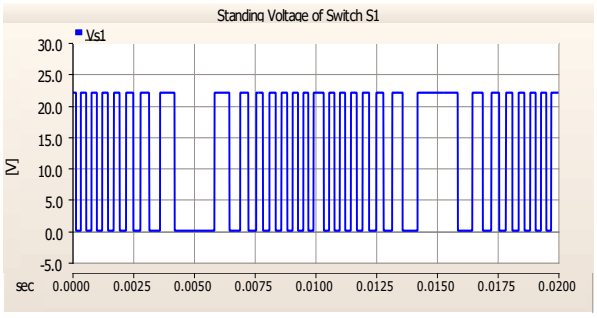


Figure 8. Output current

We have 4 switches, which are bidirectional, S_5, and S_6, from the graph, they have positive and negative standing voltages showing they are bidirectional switches. S_{11} and S_{12} are also bidirectional switches with positive and negative values. The standing voltage for S_5 and S_{11} is 88V, and for S_6 and S_{12} it is 176V, while all the other switches have zero or positive values, indicating they are unidirectional switches.



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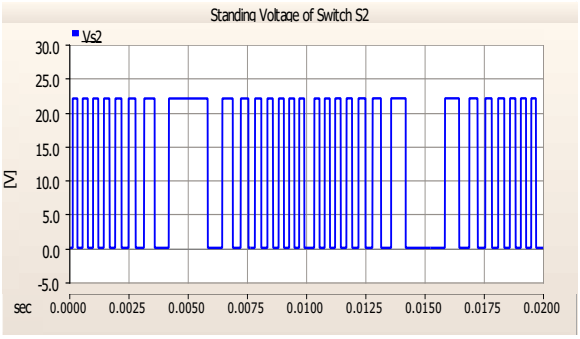

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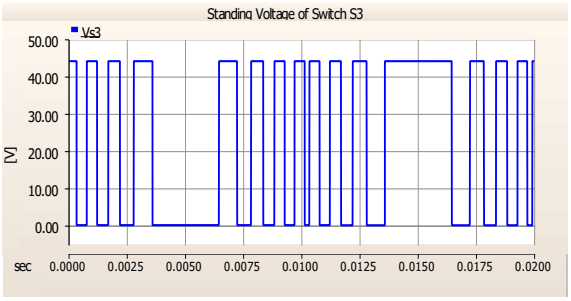

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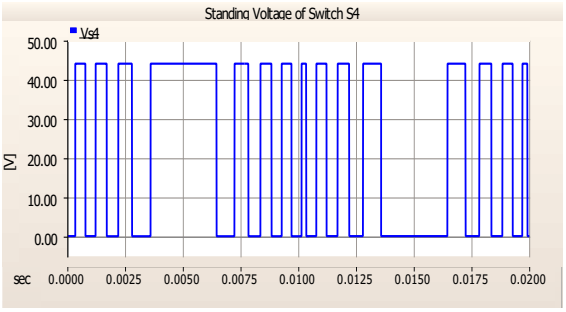

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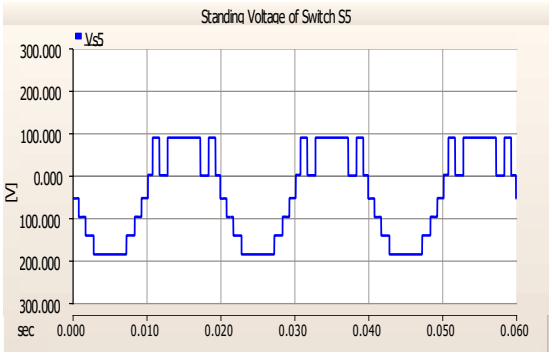

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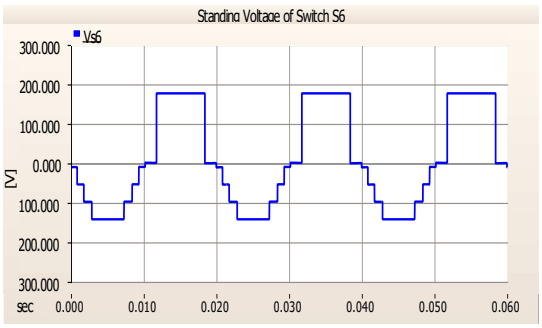

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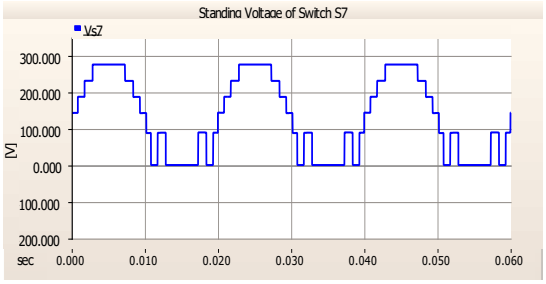

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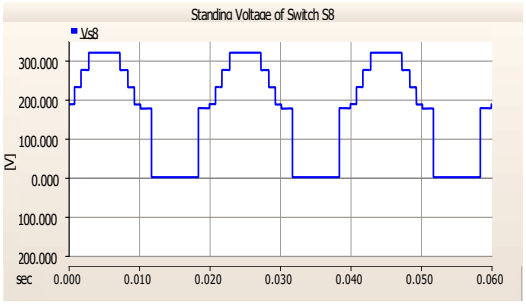

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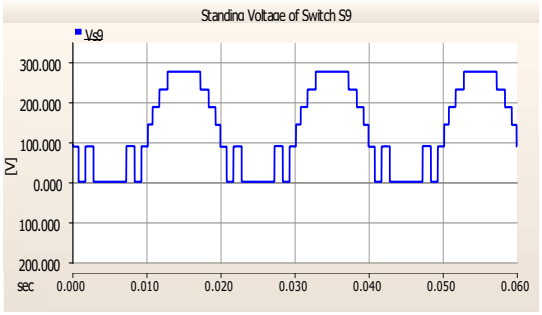

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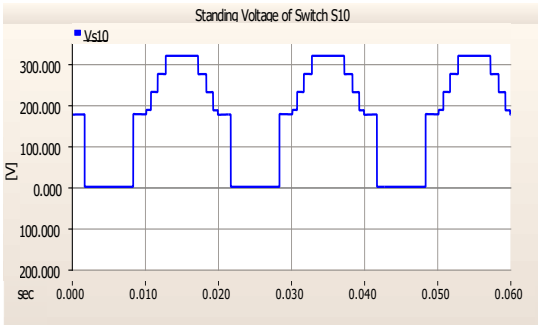

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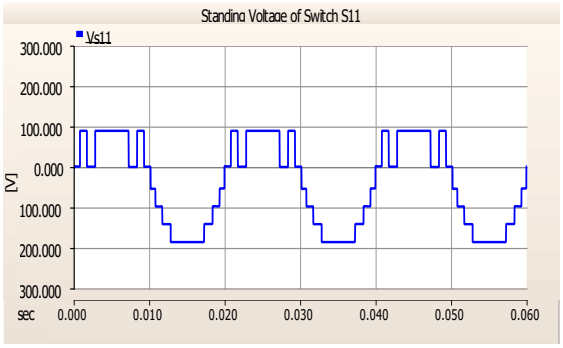

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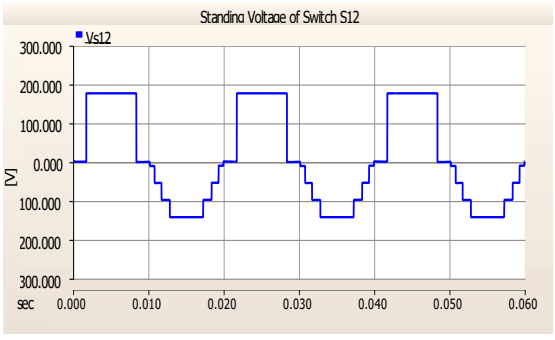

(l)

Figure 9. Standing voltages of the switches: from S_1 to S_{12}

The simulation results metrics of the 31-level inverter are shown in Table 6. The output waveforms are high quality and align with the reference signal. The efficiency of the inverter is 95.39%, with a *THD* of approximately 2%. The peak output voltage is 330V and 6.35A for the current.

Table 6. Output Simulation Metrics

Parameter	Value
Output Level	31
Peak Output Voltage, V	330 V
Load Current, A	6.35 A
Efficiency	95.39%
THD	2%

7. CONCLUSIONS

This paper proposes an enhanced single-phase H-bridge multilevel inverter for efficient renewable energy conversion to have high voltage levels, good performance, and fewer devices. The proposed topology is an improved one of that conventional H-bridge, it generates 31 voltage levels using 12 semiconductor power switches, 4 of which are bidirectional and 6 DC sources. The structure of the topology has two extra switches connected to the upper and lower parts of the topology, with 2 DC sources in each section. Analysis of the symmetric and asymmetric configurations is done, the symmetric topology generates less output voltages with the same devices in the circuit. The symmetric topology generated nine voltage levels, while the asymmetric topology was able to generate 31 levels. The presented topology is compared to other existing topologies, the presented topology is among the topologies with the lowest components, generating higher voltage levels and quality output voltage waveform.

The incremented step voltage is 22V, and the maximum output voltage of the inverter is 330V near the peak voltage of the AC supply. The control method that was used is the fundamental frequency control method; it has advantages over other methods: it is simpler to implement, and the switching losses are reduced in contrast to other control methods. The results of the asymmetric H-bridge MLI are illustrated, showing the quality of the output voltage aligning better with the reference sine waveform. The waveform of the load current is given, as well as the standing voltages of the switches.

To highlight the practical use of the proposed inverter, consider a case study in a solar power system where it converts the DC output from photovoltaic panels into AC voltage for grid connection. The inverter's 31-level output enhances voltage, minimizes losses, and provides a cleaner power output with reduced grid disturbances. Furthermore, the asymmetric design reduces the number of components needed and reduces the installation area compared to conventional topologies. Thus, it becomes a cost-effective solution for solar farms with large power needs. Simulation results show that the inverter achieves high efficiency due to its high-quality waveform and lower standing voltages on the switches. Also, incorporating advanced materials in the devices achieves higher efficiency, more than 95%.

In addition to its role in renewable energy, the proposed inverter could enhance power quality in distribution systems. In addition, its integration with smart grid technologies can address power management and stability issues, enhancing its role in future grid compatibility and power quality initiatives.

This simulation design employs standard semiconductor components; however, incorporating wide-bandgap technologies like silicon carbide (SiC) or gallium nitride (GaN) could enhance future iterations. These materials provide enhanced thermal conductivity, lower switching losses, and improved efficiency, making them especially advantageous for high-power applications. They could boost the inverter's performance, potentially lowering operational costs and enhancing reliability. Considering these advancements in future designs could lead to better energy performance and suitability for higher power demands.

Further improvement is exploring machine learning control algorithms, enabling the inverter to adjust its switching patterns dynamically based on load conditions for improved performance.

NOMENCLATURES

V_T: Voltage component of the transistor
R_T: Resistive component of the transistor
V_D: Voltage component of the diode
R_D: Resistive component of the diode
β: Constant, dependent on semiconductor switch type
E_{on}: On the state
E_{off}: Off state
T_{on}: On period of time
T_{off}: Off period time
f_s: Switching frequency
P_{SW}: Total switching losses
I: Current during on-state
I': Current during off-state
V_{SW}: Voltage of the switch in off-state

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