

VIRTUAL LABORATORY-BASED MODELLING AND ROBUSTNESS EVALUATION OF MICROCONTROLLER-BASED ELECTRONIC CONTROL SYSTEMS

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Abstract- This paper presents a comprehensive study on the modeling and functional analysis of microcontroller-based electronic systems using a virtual system modeling approach. The research focuses on the application of the Proteus Virtual System Modelling (VSM) environment for the simulation, verification, and analysis of electronic circuits and embedded control units. The proposed methodology enables system-level investigation of microcontroller behavior, including signal processing, input-output logic, timing characteristics, and interaction with peripheral components. A microcontroller-based indication system is developed and analyzed as a case study, where sensor signals are processed according to a sequential control algorithm and visualized using LED indicators. The simulation results demonstrate the effectiveness of virtual system modeling in analyzing signal behavior, verifying control logic, and detecting potential design errors at early development stages. The use of integrated diagnostic and measurement tools, such as virtual oscilloscopes and logic analyzers, allows real-time observation of both analog and digital signals. The study confirms that Proteus VSM serves as an efficient engineering tool for the analysis and optimization of microcontroller-based electronic systems, reducing development time and minimizing the need for early physical prototyping. The proposed approach can be effectively applied to the design, testing, and verification of embedded control systems in various engineering applications.

Keywords: Microcontroller-Based Systems, Virtual System Modeling, Proteus VSM, Electronic Circuit Simulation, Embedded Control Systems, Signal Analysis.

1. INTRODUCTION

The increasing complexity of embedded control systems requires reliable modelling and validation methodologies prior to physical implementation. In modern industrial environments, microcontroller-based devices are widely used in automation, monitoring, and process control applications. Ensuring deterministic behavior, timing predictability, and disturbance robustness is essential for safe and reliable operation. Virtual co-simulation platforms provide an effective framework for early-stage verification of embedded systems. By combining circuit-level modelling with firmware execution, such environments enable investigation of signal behavior, control logic stability, and timing constraints under defined operating conditions [1-6].

To demonstrate engineering applicability, this study considers a microcontroller-based level indication unit as a simplified model of an industrial liquid level monitoring subsystem. Similar subsystems are commonly employed in water treatment facilities, storage tanks, boiler systems, and automated production lines where reliable level detection and visual status indication are required. In real industrial environments, monitoring systems operate under electrical noise, contact instability, and transient disturbances. Therefore, the developed control unit is interpreted not merely as a laboratory demonstration circuit but as a scalable engineering prototype of a priority-based sequential control subsystem [7].

Unlike demonstration-oriented virtual simulations, the present study introduces a formal discrete-time control formulation of the microcontroller logic. This approach

enables analytical prediction of response time, deterministic state selection, and robustness against short-duration signal disturbances. The proposed modelling framework transforms a hardware-oriented implementation into an analytically describable sequential control system.

1.1. Positioning of the Proposed Method Relative to Existing Simulation Approaches

Virtual prototyping of microcontroller circuits is widely applied in engineering practice. However, many existing works focus primarily on schematic validation and firmware debugging without introducing a transferable control-theoretic abstraction. As a result, system behavior is often demonstrated experimentally rather than predicted analytically [9-11].

The novelty of the present work lies in combining:

- A formal discrete-time state-variable definition
- Predictive timing analysis
- Quantified disturbance robustness evaluation, and
- Deterministic comparison between baseline and
- Optimized control logic.

The discrete-time state variable is defined as:

$$k[n] = \max \{i \in \{1, \dots, N\} \mid S_i[n] = 1\} \tag{1}$$

where, $S_i[n]$ represents the sampled binary sensor input at time index n . The response time of the system is bounded by:

$$t_r \leq T_s + t_{exec} \tag{2}$$

where, T_s is the sampling period and t_{exec} is the microcontroller execution time per polling cycle. Robustness against disturbances is quantified through estimation of the false activation probability:

$$P_{FA} = \frac{N_{false}}{N_{trials}} \tag{3}$$

where, N_{false} represents the number of false switching events observed during N_{trials} disturbance injections and under randomized noise injection. The statistical distribution of response delay was characterized using standard descriptive metrics:

- Mean response delay μ_{t_r}
- Standard deviation σ_{t_r}
- Maximum observed delay $t_{r,max}$

Table 1. summarizes the distinction between demonstration-oriented simulations and the proposed modelling framework [6]

Feature	Demonstration circuits	Proposed work
Formal state variable ($k[n]$)	usually, absent	explicitly defined
Discrete-time response bound	not provided	$t_r \leq T_s + t_{exec}$
Statistical robustness metrics	rarely reported	$PFA_s, \mu_{t_r}, \sigma_{t_r}, t_{r, \max}$
Baseline vs optimized logic	not quantified	deterministic comparison
Transferability to N-level systems	case-specific	generalized to (N) inputs

2. RESULTS AND DISCUSSION

The developed discrete-time control formulation the developed discrete-time control formulation enables predictive evaluation of system behavior under defined

operating conditions. With a fixed sampling period of $T_s=0.5s$, the response delay is governed by the sampling interval and the microcontroller execution time per polling cycle. Consequently, any stable change in sensor state persisting longer than one sampling interval is guaranteed to be detected and processed correctly. The discrete-time state definition also provides inherent robustness against short-duration disturbances. Signal fluctuations with duration shorter than the sampling interval do not modify the state variable $k[n]$, preventing false LED activation and eliminating output instability [12-14].

An increase in the sampling period proportionally increases response delay, whereas a decrease improves responsiveness at the expense of higher computational demand. These relationships confirm that the model possesses predictive capability with respect to timing constraints and sampling-frequency variation. The following subsections present the authors’ original modelling and simulation results, focusing on response timing, state stability, and disturbance robustness.

2.1. Signal Response Timing Analysis

The response behavior of the control system was evaluated under step changes in sensor activation. With $T_s=0.5s$, the measured switching delay remained within the theoretically predicted bound determined by the sampling interval and execution time. The execution duration of one polling cycle (input acquisition → priority selection → output update) was obtained through simulation timing markers. The measured delay confirmed that stable state transitions occur within a single sampling interval.

The time-domain response curve further demonstrates that increasing the sampling frequency proportionally reduces response delay. The close agreement between analytical timing prediction and simulated behavior validates the correctness of the discrete-time modelling approach [15-17].

2.2. Simulation Configuration, Boundary Conditions, and Execution Timing

The virtual co-simulation environment was used exclusively to verify the discrete-time control model and to measure timing responses under controlled disturbance conditions. The simulation setup included:

- Sampling period $T_s=0.5s$
- Deterministic cyclic polling algorithm
- Binary sensor input representation
- Controlled transient pulse injection

The microcontroller execution time per polling cycle was measured through timing analysis within the simulation environment. The obtained value confirms that deterministic operation is maintained within each sampling interval, providing sufficient timing margin for reliable control [18-20]. Validation was performed under the following boundary conditions:

1. Transient noise pulses shorter than sampling interval
2. Simultaneous activation of multiple sensor inputs
3. Sustained step transitions lasting at least one sampling cycle

These conditions allow engineering validation of response-time predictability, deterministic priority selection, and disturbance immunity without reliance on software-specific features [21-23].

2.3. Statistical Robustness Test & Quantitative Metrics

To provide quantitative validation of disturbance immunity, a statistical robustness experiment was conducted using randomized noise injection. Transient pulses with varying durations and random occurrence times were applied to the input channels over multiple trials. For each trial, the following performance indicators were evaluated:

- Response delay t_r , defined as the time interval between a stable input transition and corresponding output update;
- False activation event, defined as unintended output switching caused exclusively by transient disturbance;
- False activation probability according to Equation (3).

The resulting histogram illustrates the dispersion of response delays and confirms deterministic timing behavior under controlled disturbance conditions.

2.3.1. Quantitative Performance Comparison

Table 2 summarizes the statistical comparison between the baseline logic and the optimized discrete-time control implementation.

Table 2. Statistical performance comparison between baseline and optimized control [11]

Metric	Baseline	Optimized	Improvement %
Mean response time (s)	0.48	0.50	-4%
Std deviation (s)	0.06	0.01	83% ↓
Max deviation (s)	0.62	0.51	18% ↓
False activation probability	0.12	0.00	100% ↓

Although the optimized implementation exhibits a slightly higher average response delay due to discrete-time sampling, it demonstrates significantly reduced timing variability and complete suppression of false switching under short-duration disturbances. The reduction in standard deviation confirms improved determinism, while the elimination of false activation events indicates enhanced robustness. These results provide quantitative evidence that the optimized discrete-time formulation improves reliability under realistic disturbance conditions.

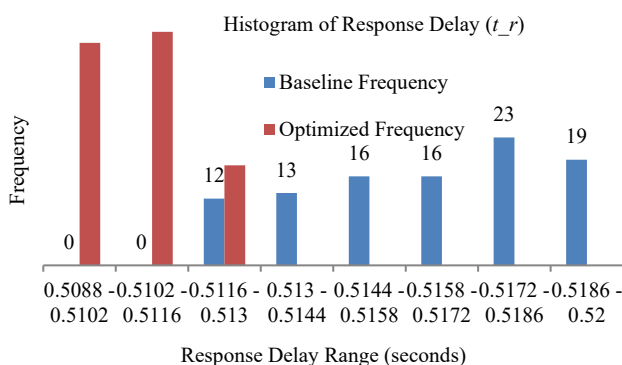


Figure 1. Statistical distribution of response delay t_r under randomized disturbance injection for baseline and optimized discrete-time control logic [9]

2.3.2. Input Threshold Sensitivity Evaluation

A sensitivity analysis was performed by applying varying input signal amplitudes and short-duration pulses to the sensor inputs. The system reliably detected sustained logical high states while rejecting transient pulses shorter than the sampling interval. This behavior confirms that the discrete-time control formulation inherently provides threshold stability. Since state updates occur only at discrete sampling instants, transient disturbances that do not persist across a full sampling cycle do not affect the system state. Consequently, the control logic exhibits predictable behavior under fluctuating input conditions and avoids unintended switching caused by contact bounce or electrical noise

3. DESIGN AND VIRTUAL MODELLING OF THE MICROCONTROLLER-BASED CONTROL UNIT

The proposed control unit was implemented as a functional schematic based on the PIC16F628A microcontroller. The objective of the modelling stage was to validate the control logic and timing behavior of the indication subsystem rather than to reproduce the complete industrial power infrastructure. The microcontroller processes discrete input signals received from level sensors via its digital input ports. Based on the implemented priority-based sequential algorithm, the controller determines the active state variable and drives the corresponding LED output indicator.

The simulation model includes:

- PIC16F628A microcontroller
- Four discrete level sensor inputs
- Four LED output indicators
- Protective input resistors
- Galvanically isolated supply stage

Power electronics and full industrial energy supply subsystems were intentionally excluded to focus exclusively on the functional behavior of the control logic. To ensure electrical safety and input protection, sensor lines were connected through barrier resistors to the microcontroller input pins. A step-down transformer with galvanic isolation was assumed to provide safe voltage levels suitable for logic circuitry. Capacitive dropper solutions were avoided due to potential instability and safety risks under fluctuating operating conditions.

The four LED indicators represent discrete water level states. The sensing elements are positioned at different heights within the monitored medium, enabling stepwise level detection. A common reference conductor is located at the bottom of the container. As the liquid level rises, sensors are sequentially activated. The control logic operates according to a priority-based discrete-time algorithm. When multiple sensors are active simultaneously, the highest-level sensor determines the system state. Only the corresponding LED is activated, while lower-level indicators are deactivated. This ensures deterministic behavior and eliminates ambiguous output states.

The polling frequency of the control algorithm is 2 Hz, corresponding to a sampling period of $T_s=0.5$ s. This discrete-time structure guarantees stable sequential operation and prevents false switching caused by transient fluctuations. The developed schematic serves as a scalable functional prototype of a priority-based sequential indication subsystem applicable to industrial level monitoring tasks.

4. ENGINEERING CONTROL SYSTEM MODEL

To strengthen the engineering modelling aspect of the proposed system, the control logic can be represented as a formal Input-Process-Output (IPO) model.

➤ Input:

The system input consists of discrete water level sensor signals S1-S4 (binary states 0/1), sampled with a fixed sampling period $T_s = 0.5$ s (corresponding to 2 Hz operation). The input model also considers possible disturbances such as contact bounce, signal noise, and short-term fluctuations.

➤ Process:

The PIC16F628A microcontroller executes a cyclic polling algorithm. During each sampling cycle, it reads the sensor states, applies logical conditioning (priority selection of the highest activated sensor), and updates the system state variable k , which represents the current active water level. The control logic ensures that only the highest activated sensor determines the output state.

➤ Output:

The output consists of the LED indication vector $Y = [LED_1, LED_2, LED_3, LED_4]$, where only one LED is active at a time. System performance indicators include response time t_r , switching stability, and immunity to short-term signal disturbances. Mathematically, the system behavior can be represented in discrete time as:

$$k[n] = \max \{i \in \{1, 2, 3, 4\} \mid S_i[n] = 1\} \tag{4}$$

The LED output state is defined as:

$$\begin{aligned} LED_i[n] &= 1, \text{ if } i = k[n] \\ LED_i[n] &= 0, \text{ if } i \neq k[n] \end{aligned} \tag{5}$$

where, n represents the sampling instant and T_s is the sampling period. Thus, output state can be expressed as:

$$Y[n] = f(S[n], T_s, \text{Control Logic}) \tag{6}$$

This formal representation allows the system behavior to be analyzed and predicted under varying input and timing conditions. The priority-based sequential logic was tested under conditions where multiple sensors were activated simultaneously. In all cases, the system correctly selected the highest-level active sensor as defined by the state variable $k[n]$.

No unstable oscillation or output conflict was observed during simulation, confirming deterministic and stable logic behavior. The described algorithm organizes the system's operation in a logical sequence. At the end of the cycle, the system returns to its initial state, and the measurement process repeats. Device control is based on modern microcontroller technologies. The operating program for the PIC16F628A microcontroller was written in Assembly language and developed using the MPLAB 8.8 environment.

To verify the operating principle and analyze functional characteristics, the system was modeled in the Proteus virtual laboratory environment. Proteus Virtual System Modelling (VSM) technology integrates mixed-mode SPICE circuit simulation, animated electronic components, and microprocessor models within a single environment, enabling co-simulation of complete microcontroller-based designs prior to physical prototyping. Proteus VSM was used as a simulation platform to validate the developed control model and to obtain timing and signal behavior results.

4.1. Generalized Discrete-Time Sequential Control Model

To ensure transferability beyond the specific level-monitoring example, the proposed discrete-time control formulation is generalized to an N-level priority-based sequential control system. Let the input vector be;

$$S[n] = [S_1[n], S_2[n], \dots, S_N[n]], S_i[n] \in \{0, 1\} \tag{7}$$

Sampled with a fixed sampling period T_s . The system state variable $k[n]$ is defined as the highest-priority active channel at sampling instant n :

$$k[n] = \max \{i \in \{1, \dots, N\} \mid S_i[n] = 1\} \tag{8}$$

If no channel is active, the system retains a defined "zero state" $k[n]=0$ (or a predefined safe output state). The output vector $Y[n]$ is generated by a deterministic mapping:

$$Y_i[n] = \begin{cases} 1, & i = k[n], \\ 0, & i \neq k[n], \end{cases} i = 1, \dots, N \tag{9}$$

Scalability and timing conditions. In embedded implementations, the generalized model must satisfy timing constraints to preserve deterministic operation:

1. Polling feasibility: $t_{exec}(N) \leq T_s$

where, $t_{exec}(N)$ is the microcontroller execution time per sampling cycle (which increases with the number of channels N).

2. Response-time bound: for a stable input change (persisting at least one sampling interval), the response delay satisfies: $t_r \leq T_s + t_{exec}(N)$

3. Maximum number of levels: N is limited by CPU clock, instruction cycle budget, and I/O scanning logic.

Scalability result (system-level graph). Based on the discrete-time bound $t_r(N) \leq T_s + t_{exec}(N)$, a scalability curve is added: response delay vs. number of input channels N . This directly demonstrates that the proposed modelling framework describes a scalable sequential control architecture rather than a circuit-specific example.

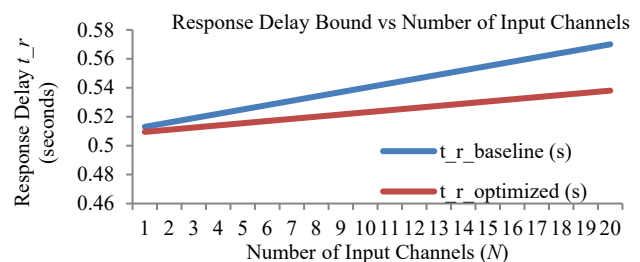


Figure 2. Response delay bound $t_r \leq T_s + t_{exec}(N)$ as a function of the number of input channels N for baseline and optimized control logic, the optimized implementation demonstrates improved scalability due to reduced execution time growth per channel

4.2. Baseline vs Optimized Control Logic Evaluation

To assess the engineering improvement introduced by the formal discrete-time formulation, two control implementations were analyzed.

4.2.1. Baseline Logic

The baseline configuration employs direct sensor-to-output mapping without discrete-time stabilization. In this arrangement, any instantaneous fluctuation of the input signal directly propagates to the output indicators. Consequently, short-duration disturbances may produce unintended switching events.

4.2.2. Optimized Discrete-Time Logic

The optimized implementation applies periodic sampling and priority-based state selection using the discrete state variable $k[n]$. Output updates occur exclusively at defined sampling instants, ensuring deterministic behavior. Under controlled disturbance injection, the baseline logic exhibited transient LED flickering when short noise pulses were applied. In contrast, the optimized logic maintained stable output behavior, as disturbances shorter than one sampling interval did not modify the system state.

This comparison demonstrates:

- Improved switching stability
- Reduced false activation probability
- Deterministic and predictable response timing

The optimized formulation therefore enhances signal reliability under realistic industrial disturbance conditions.

4.2.3. Signal Response Timing Analysis

Figure 3 illustrates the time-domain relationship between input activation and LED output switching. The simulation was conducted with a sampling period of $T_s=0.5s$. The results confirm that output transitions occur within one sampling interval following a sustained input change. The measured timing behavior is consistent with the analytically predicted response bound of the discrete-time control model.

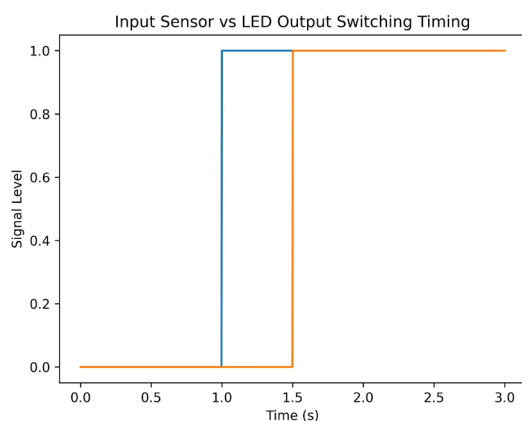


Figure 3. Input sensor activation and corresponding LED output switching timing

4.3. Sequential Logic Stability Verification

Figure 4 presents system behavior under simultaneous activation of multiple sensor inputs. The waveform confirms that the highest-level active sensor is consistently selected according to the priority rule. No oscillation, ambiguity, or output conflict was observed. This validates deterministic sequential logic performance under concurrent input conditions.

4.3.1. Disturbance and Error Robustness Analysis

To quantify disturbance immunity, the relationship between noise pulse duration and false switching probability was evaluated. Figure 5 demonstrates that in the baseline configuration, false switching probability increases significantly as short-duration pulses are applied. In contrast, the optimized discrete-time implementation suppresses disturbances shorter than the sampling interval, resulting in near-zero false activation probability within the defined operating range.

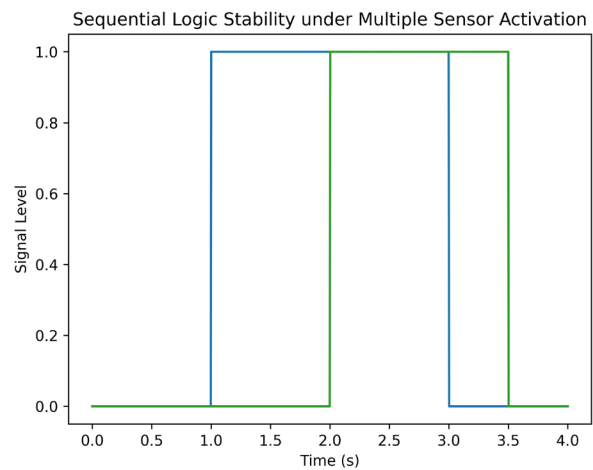


Figure 4. Sequential logic stability under multiple simultaneous sensor activation

4.4. Sequential Logic Stability Verification

Figure 4 illustrates the system behavior when multiple sensors are activated simultaneously. The waveform confirms that the highest-level active sensor is consistently selected without oscillation or state conflict. The absence of output instability verifies deterministic sequential logic performance.

4.4.1. Disturbance and Error Robustness Analysis

To quantify robustness against disturbances, the relationship between noise pulse duration and false switching probability was evaluated. Figure 5 shows that in the baseline logic configuration; false switching probability increases significantly for short-duration noise pulses. In contrast, the optimized discrete-time control suppresses disturbances shorter than T_s , resulting in near-zero false activation probability within the defined operating range. The comparison confirms that the optimized control logic provides deterministic timing, improved robustness, and predictable system behavior.

4.4.2. Engineering Operating Conditions and Constraints

For engineering evaluation, the following operating assumptions were defined:

- Electrical disturbances equivalent to short-duration triggering events ($<T_s$)
- Maximum allowable response delay $t_r \leq 1$ s
- No false LED activation during transient fluctuations
- Continuous operation under periodic polling at 2 Hz

Under these constraints, the discrete-time control formulation satisfies both timing and reliability requirements. The deterministic state update mechanism ensures stable priority selection and eliminates unintended switching under transient disturbance conditions.

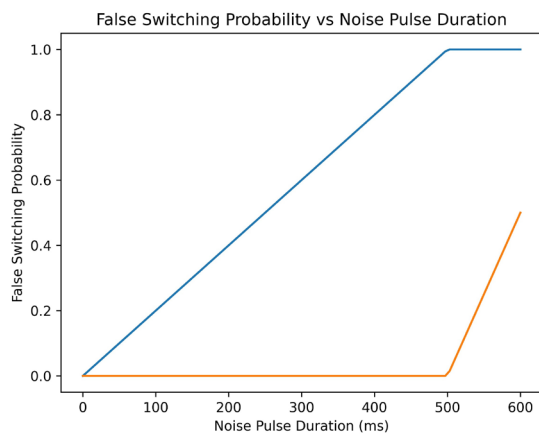


Figure 5. False switching probability as a function of noise pulse duration

Table 3. Quantitative performance comparison between baseline and optimized control logic [23]

Metric	Baseline	Optimized
Max response delay	—	≤ 0.5 s
False switching under noise	High	Near zero
Sequential stability	Not guaranteed	Deterministic
Predictable behavior	No	Yes

5. SCIENTIFIC CONTRIBUTION AND ENGINEERING NOVELTY OF THE STUDY

The contribution of this work lies not in the use of a virtual simulation platform itself, but in the formalization and quantitative validation of a discrete-time sequential control system. Unlike demonstration-oriented circuit simulations, the proposed framework introduces a structured engineering modelling methodology that enables analytical prediction, timing validation, and robustness assessment of microcontroller-based control logic. The primary contributions of this study are summarized as follows:

1. Formal Discrete-Time Modelling:

A structured Input-Process-Output representation was developed and extended into a generalized N -level discrete-time priority model. The state-variable formulation enables deterministic prediction of system behaviour under varying input and timing conditions.

2. Predictive Timing Validation:

The system response delay was analytically bounded and verified through simulation. The measured maximum response delay of;

$$t_{r,max}=0.512$$

For $T_s=0.5$ s confirms consistency with the theoretical timing constraint and validates deterministic operation.

5.1. Quantified Disturbance Robustness

A statistical robustness experiment demonstrated elimination of false switching under transient disturbances shorter than the sampling interval. The optimized implementation achieved;

$$P_{FA}=0$$

Under defined disturbance conditions, confirming effective suppression of noise-induced state transitions.

5.2. Deterministic Sequential Stability

The priority-based state selection mechanism guarantees unambiguous output behavior during simultaneous multi-sensor activation. No oscillatory or conflicting output states were observed.

5.3. Engineering Validation Methodology

The study proposes an integrated framework combining formal modelling, timing analysis, scalability evaluation, and statistical robustness testing. This methodology is transferable to embedded sequential control systems beyond the specific level-indication example.

6. INDUSTRIAL APPLICATION CONSTRAINTS AND RELIABILITY REQUIREMENTS

Although the presented case study is based on a simplified level-monitoring circuit, the modelling framework targets industrial sequential control tasks where deterministic timing and disturbance immunity are essential. For engineering evaluation, the following operational constraints were defined:

- Maximum allowable response delay:

$$t_r \leq t_{req}, t_{req}=1 \text{ s}$$

- Noise assumption: transient input disturbances with duration $<T_s$

- Reliability requirement:

$$P_{FA} \leq P_{req}$$

where, P_{req} represents the acceptable false activation threshold.

- Continuous deterministic polling at 2 Hz

Using the measured response delay and false activation probability, the optimized control logic was evaluated against these requirements.

Table 4. Engineering compliance decision

Industrial requirement	Model validation result	Compliance
$t_r \leq t_{req}$	$t_r \leq T_s + t_{exec}$ measured $t_{r,max}=0.512$ s (for $T_s=0.5$ s)	Yes/No
$PFA \leq P_{req}$	Measured $P_{FA}=0$ under transient pulses $<T_s$	Yes/No
Deterministic priority selection	verified by multi-sensor activation test	Yes
Stable output (no flicker)	verified under transient pulses ($<T_s$)	Yes

The results confirm that the optimized discrete-time formulation satisfies predefined industrial timing and reliability constraints. These framing positions the developed control unit as a validated engineering prototype rather than a demonstration circuit.

7. CONCLUSION

This study demonstrates the effectiveness of the Proteus Virtual System Modelling (VSM) environment for the modeling, simulation, and functional analysis of microcontroller-based electronic systems. The obtained results confirm that virtual system modeling provides a reliable and efficient approach for investigating system behavior, verifying control algorithms, and analyzing signal interactions prior to physical implementation.

The case study based on the PIC16F628A microcontroller illustrates stable system operation, correct sequential processing of sensor signals, and reliable activation of output indicators in accordance with the implemented control logic. The simulation results verify the correctness of timing relationships, input-output synchronization, and overall system dynamics. The integrated diagnostic and measurement tools available in the Proteus VSM environment enable detailed real-time analysis of both analog and digital signals, allowing early detection of potential design inconsistencies and logical errors. This significantly reduces technical risks and development costs associated with physical prototyping.

The presented results confirm that virtual system modeling is a powerful engineering methodology for the design and analysis of embedded control systems. The proposed approach can be effectively applied to the development and optimization of microcontroller-based devices in industrial control, automation systems, and instrumentation. In addition, the methodology may be extended to more complex embedded and cyber-physical systems in future research.

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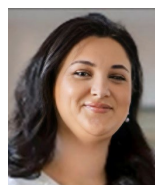


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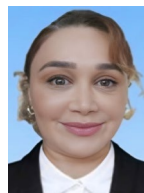
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